八十四學年度 粒子工程与工程物理 所 組碩士班研究生入學考試

科目 電子學 科號 309 共 3 頁第 1 頁 *請在試卷【答案卷】內作答

1. Does the barrier voltage (built–in voltage) across the depletion layer in diode appear between the metal contact terminals ? Why ? (6%)
2. Sketch the JK master–slave FLIP–FLOP by use of NAND gates.(10%)
3. (a) For the voltage transfer curve of a CMOS inverter shown in the Fig.3, what are the operation mode of Q_N and Q_P for the A, B, C, D, and E segments, respectively ? (Answer in terms of Off, or Triode, or Saturation)(10%)

   (b) Sketch the cross–section of a CMOS inverter in an IC chip.(8%)

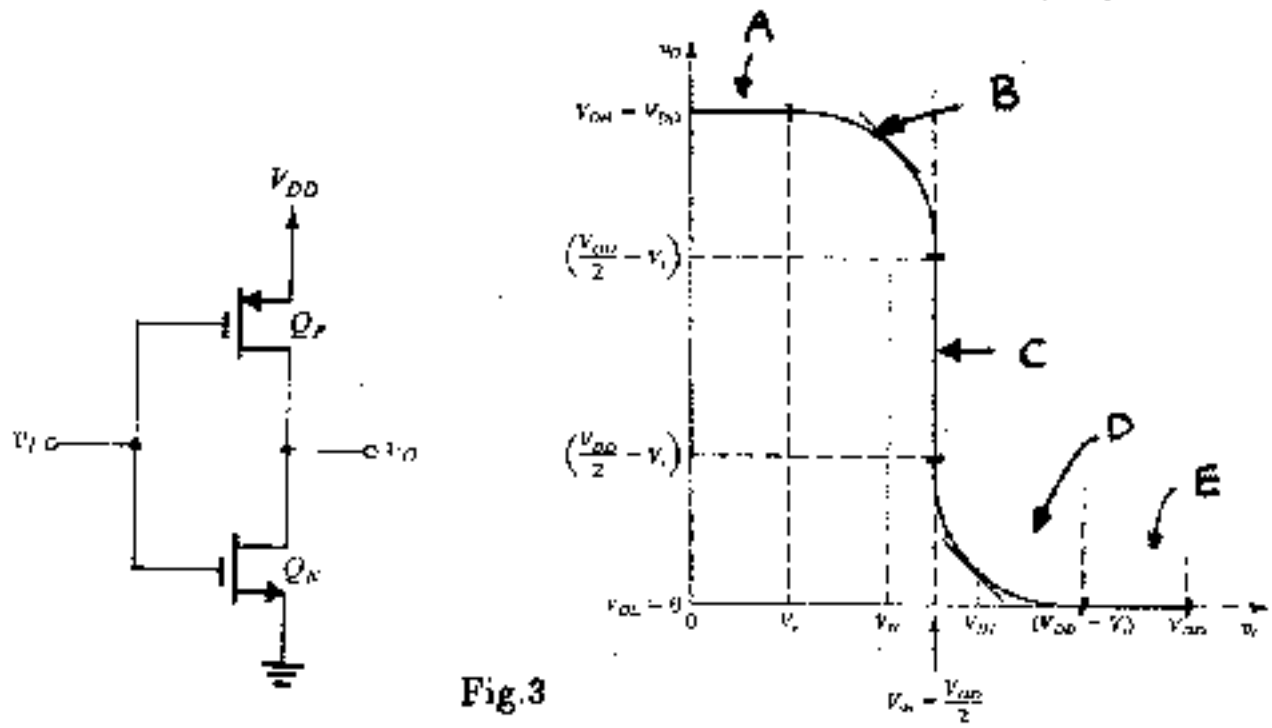


Fig.3

4. For the Fig.4, sketch the i_D and v_D waveforms corresponding to the v_I signal.(10%)

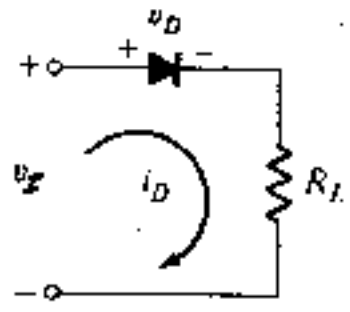
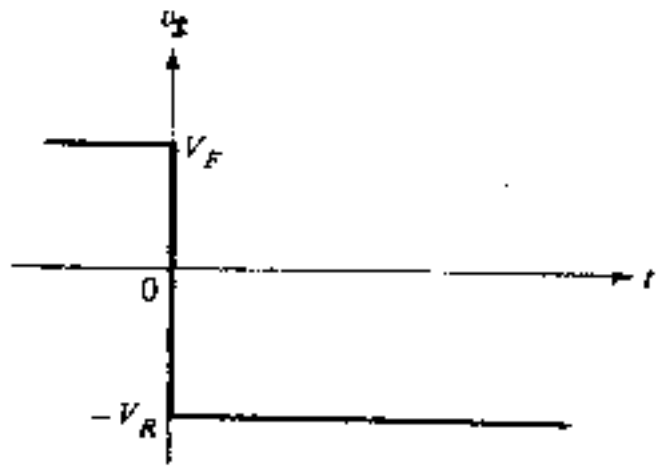


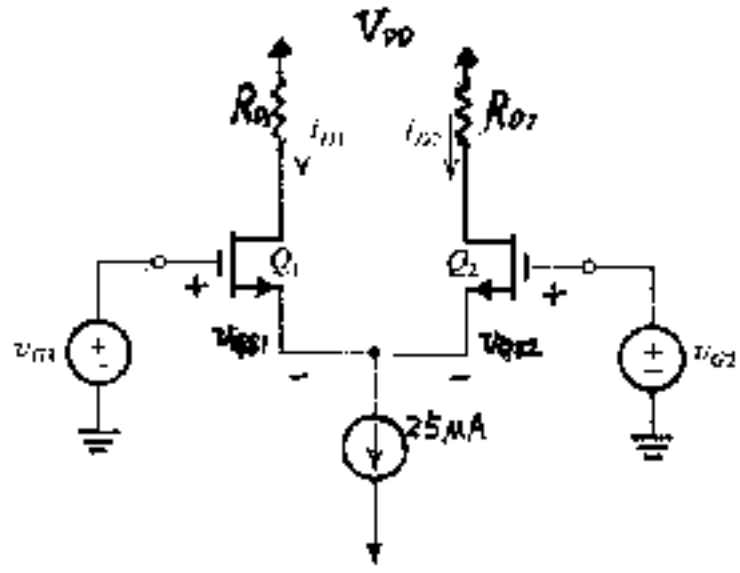
Fig.4



八十四學年度 [illegible] 所 _____ 組碩士班研究生入學考試

科目 電子學 科號 3309 共 3 頁第 2 頁 *請在試卷【答案卷】內作答

5. For the differential pair circuit of the Fig.5, the MOSFETs have $V_t = 1$ V, W/L=20, and $\mu_n C_{ox} = 20\ \mu A/V^2$. Find the V_{GS}, the i_{D1} as a function of v_{id}, and the v_{id} for full current switching.(18%)



$v_{id} = v_{GS1} - v_{GS2}$

Fig.5

6. (a) What are the advantages of cascode amplifier compared with the common–emitter amplifier ? Why ? (8%)

(b) For the Fig.6, the BJTs have hybrid–π parameters: $r_\pi = 2.5$ KΩ, $r_x(r_b) = 50\ \Omega$, $C_\pi = 13.9$ PF, and $C_\mu = 2$ PF. Find the midband gain A_M and the upper 3 dB frequency f_H. (15%)

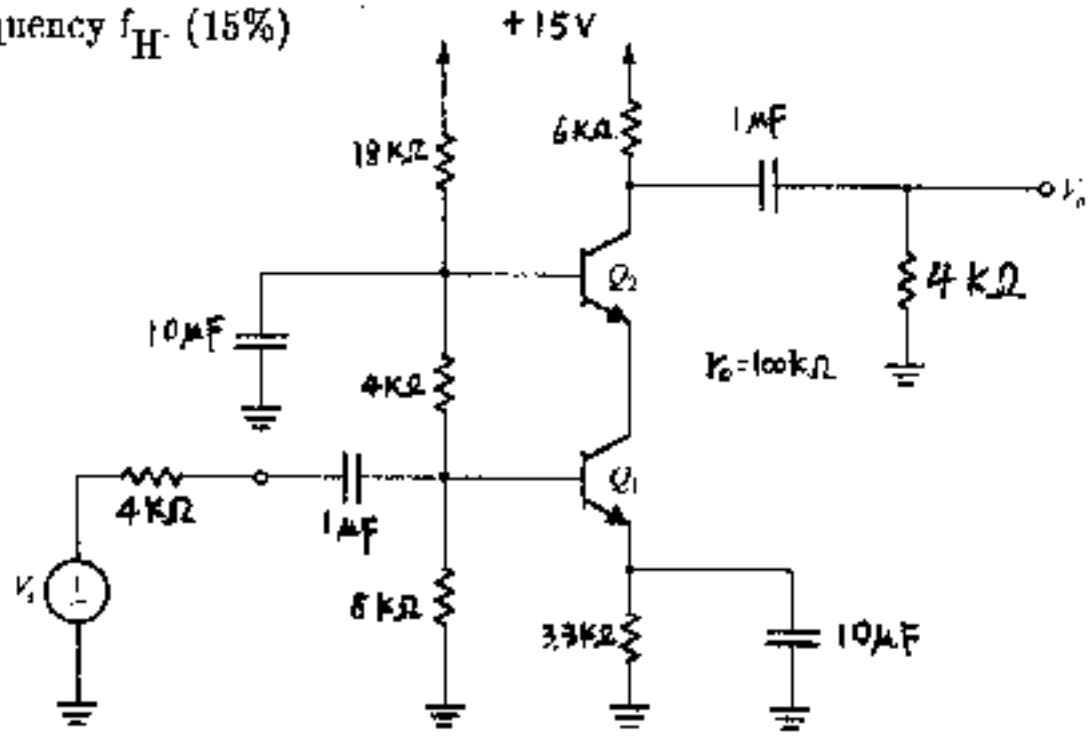


Fig.6

7. The electron concentration n(x) in a semiconductor is shown in the Fig.7.(15%)

(a) Find the electron current density $J_n(x)$ if no applied electric field

(b) Find the built–in electric field $\mathcal{E}(x)$ if $J_n(x)=0$.

(c) Find the potential between x=0 and x=W if $n(0)/n_0 = 10^3$.

(Hint: $J_n = q\mu_n n \mathcal{E} + qD_n \frac{dn}{dx}$, $V_T = \frac{D_n}{\mu_n}$)

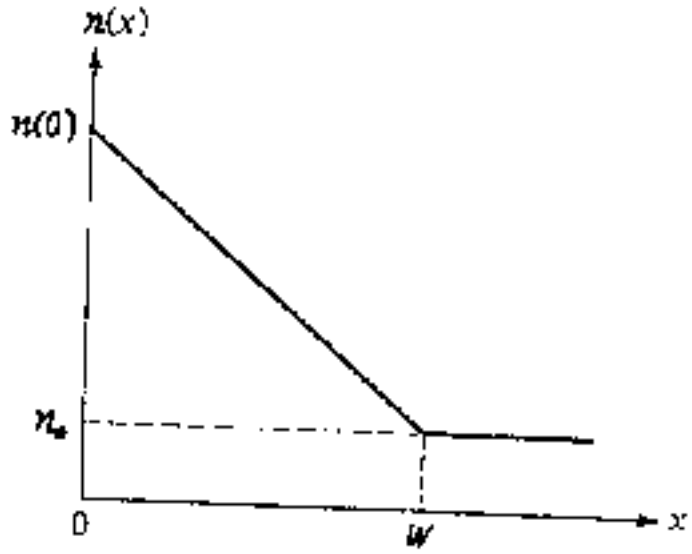


Fig.7