***** 為避免漏閱，請將各大題之答案依順序寫在一起 *****

1.

In the circuit as shown, the junction diode D_1 can be modeled by a forward constant voltage drop of $V_\gamma = 0.7$ V; the zener diode D_2 can be modeled by an ideal zener voltage of $V_z = 3.3$ V; the op-amp is ideal; the BJT has parameters $\beta = 50$, $V_{BE(on)} = 0.7$ V, $V_A = \infty$, $V_{CE(sat)} = 0.5$ V. The resistors are $R_1 = R_2 = R_3 = R_4 = R_5 = 1$ kΩ, $R_6 = 50$ Ω. The supply voltage is $V_{CC} = 12$ V.

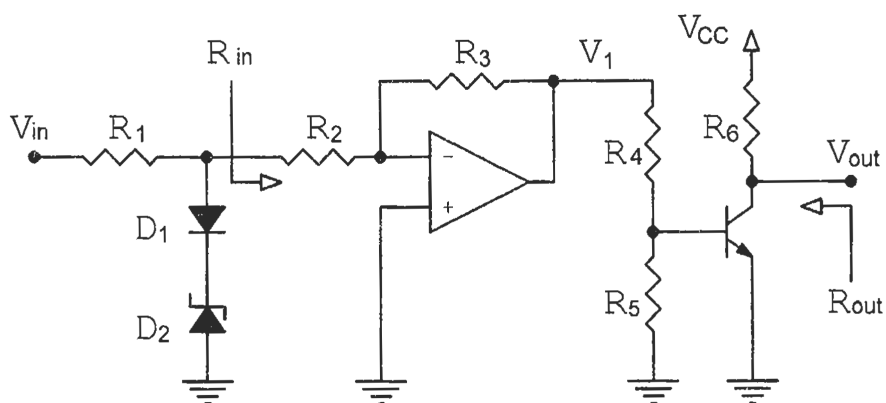
Find the voltage V_1 for $V_{in} = -10$ V, -5 V, 5 V, and 10 V. (8 %)

(a) **Derive** the expression for V_{out} as function of V_1. (4 %)

(b) **Derive** the expression for V_1 such that $V_{out} = V_{CE(sat)}$. (4 %)

(c) **Find** the value for R_{in} and R_{out}. (2 %)

(d) If V_{in} is a sinusoidal waveform with amplitude of 10 V, **sketch** the waveforms of V_{in}, V_1 and V_{out}. **Mark** proper voltage scales on your plots. (7 %)

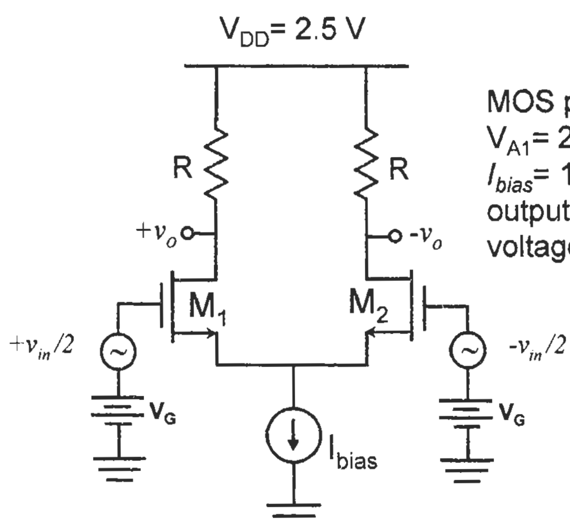


2.

(2.1) **Find** the correct statements from the following items (multiple choices, no partial credits): (5%)

(a) Intrinsic gain (A_0) of BJT totally depends on process.
(b) The gate-source capacitance in MOSFET is dominated by the overlap capacitance.
(c) Output resistance of MOSFET reduces when the gate length scales down.
(d) Input impedance of MOSFET is infinity at high frequencies.
(e) BJTs have higher gain but lower linearity than MOSFETs.

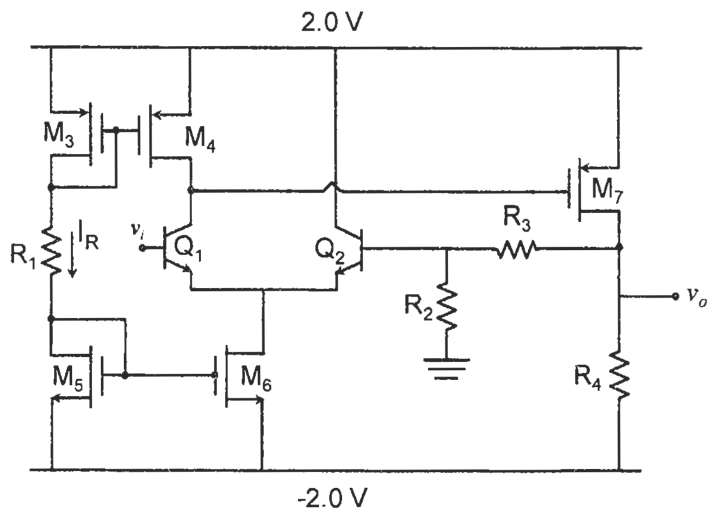
(2.2) For the circuit shown below, **find** the correct descriptions (multiple choices, no partial credits): (5%)



MOS parameters: $\mu_n C_{ox}$= 100 μA/V^2, W/L= 100, V_{A1}= 20 V (M_1), V_{A2}= 40 V (M_2), I_{bias}= 100 μA, V_{DD}= 2.5 V, R= 5 kΩ, output resistance of I_{bias}= 10 MΩ, voltage across I_{bias} is about 0.75 V.

(a) Differential gain= –5 V/V.
(b) For the single-ended output, the common mode gain= -2.5×10^{-4} V/V.
(c) For the single-ended output, |CMRR|= 86dB.
(d) v_{in} should be limited between ± 0.14 V to keep the circuit with linear amplification.
(e) Input offset voltage = 1.8 mV, when considering the V_A mismatch.

(2.3) **Find** the correct answers from the items listed below. (no partial credits, if either one of the answers in the subquestion is incorrect)



NMOS	PMOS
μ_nC_{ox}= 100 μA/V²	μ_pC_{ox}= 50 μA/V²
V_t= 0.7 V	$\lvert V_t\rvert$= 0.7 V
V_A= 40 V	$\lvert V_A\rvert$= 20 V

$(W/L)_3 = (W/L)_4 = (W/L)_5 = 100$, $(W/L)_6 = (W/L)_7 = 200$, $\beta = 50$, V_A(BJT)= 50 V

R_2= 9 kΩ, R_3= 1 kΩ, R_4= 10 kΩ

Assume v_i is set so the DC value of v_o= 0 V

(a) 6.1×10⁷	(g) 22000	(m) series-series	(s) 6.1×10⁶	(y) 1880
(b) 25900	(h) series-shunt	(n) 220	(t) shunt-shunt	(z) 2600
(c) 4760	(i) 1.11	(o) 0.9	(u) 0.11	
(d) 6.8×10⁶	(j) 26300	(p) 226	(v) 0.002	
(e) shunt-series	(k) 22600	(q) 0.1	(w) 2630	
(f) 9.0	(l) 1.8	(r) 0.18	(x) 6.8×10⁷	

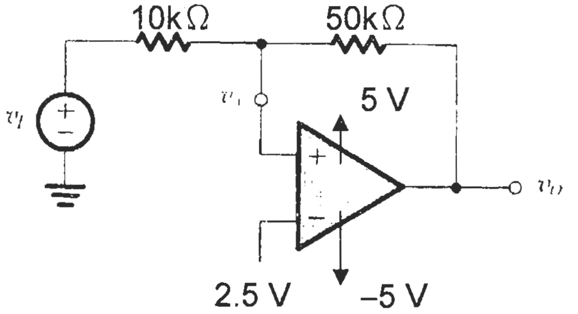
(2.3.1) The feedback type of this circuit is ___; the feedback factor is___. (5%)

(2.3.2) The value of R_1 is __ Ω so that I_R= 100 A; the low-frequency small-signal gain ($|v_o/v_i|$) is ___V/V. (5%)

(2.3.3) The output resistance of this circuit is___Ω ; the input resistance of this circuit is ___Ω. (5%)

3.

(a) For the circuit below, (a.1) **Is** this a positive or negative feedback circuit? (a.2) **Sketch** the transfer characteristic, (a.3) **Describe** its applications. (9 %)



(b) For an n-channel MOSFET operated in the saturation region, $i_D = 1/2(\mu_n Co)(W/L)(V_{GS}-V_t)^2(1+\ \lambda V_{DS})$, $\lambda = 1/V_A$, $r_o = V_A / I_D$. If the L of device is scaled to be very short, the r_o will **be** increased or decreased or unchanged ? (2 %)

(c) Following the (b), what **are** the units of μ_n and Co, respectively ? (please use cm, g, s, F, V, etc) (6 %)

(d) For a n-channel MOSFET operated in the triode region, how does the channel resistance **vary** with V_{DS}? (increased or decreased or unchanged) (2 %)

(e) For a normally-on type JFET, **is** the gate junction operated in the forward or reverse bias ? (2 %)

(f) After the floating gate of an n-channel type EPROM being programmed (charged), will the drain current **be** high or low as the memory cell is read ? (2 %)

(g) **Is** the switching capacitor circuit proposed to replace the inductor (L), capacitor (C), or resistor (R) ? (2 %)

4.

One form of NMOS circuit logics called pass transistor logic can minimize power dissipation and maximize device density. However, this logic also has some problems if circuits are not carefully designed. Consider a pass transistor logic circuit that consists of three NMOS transistors N1, N2, and N3, one output Y, and four inputs A, B, A' (the complement of A) and B' (the complement of B) with connection described below. Voltage VDD, inputs B, and B' are connected to one-end of NMOS transistors N1, N2, and N3, respectively. On the other hand, output Y is connected to another ends of NMOS transistors of N1, N2, and N3. The gates of NMOS transistors N1, N2, and N3 are, respectively, connected to input A, the same input of A, and the complement of A (=A'). Please answer the following questions.

(a) 10 % **Draw** the circuit and **mark** source/drain of the NMOS transistor(s) if known.

(b) 5% What **is** the logic function of Y that this circuit tries to implement?

(c) 5% Except smaller logic swing, what **is(are)** the potential problem(s)?

(d) 5 % How do you **modify** this circuit to avoid the potential problem(s) in (c)?