國　立　清　華　大　學　命　題　紙

96 學年度 電機領域聯合招生 系（所） 組碩士班入學考試

科目 電子學 科目代碼 9904 共 3 頁第 1 頁 *請在【答案卷卡】內作答

1. [25%] In the circuit as shown in Figure 1, the BJT can be modeled by $\beta = 100$, $r_o = \infty$ and $V_{BE(on)} = 0.7$ V. The current source is ideal with $I_Q = 1$ mA. The zener diode is ideal with breakdown voltage $V_Z = 2.5$ V. The operational amplifier is ideal. The parameters of other components are: $R_1 = R_2 = R_3 = R_4 = 10$ kΩ; $V_{CC} = 10$ V; $V_{EE} = -10$ V. The input voltage V_{IN} is confined in a range such that the BJT is in forward active mode.
   (a) Find the minimum of input voltage range, $V_{IN,min}$.[3%]
   (b) Find the voltage V_1 for a given V_{IN}.[3%]
   (c) Determine the current I_{IN} for $V_{IN} = 3.5$ V. [3%]
   (d) Determine the current I_{IN} for $V_{IN} = 8.5$ V. [3%]
   (e) Write the expression for V_{OUT} as function of V_{IN}. [7%]
   (f) Plot the curve of V_{OUT} vs. V_{IN} for -8 V $< V_{IN} < 8$ V. Mark the proper scales in your plot. [6%]

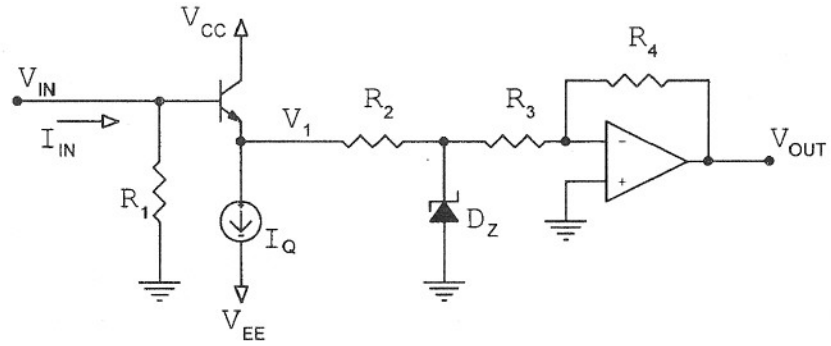

Figure 1

2. [13%] Shown in Figure 2 is the schematic of a feedback amplifier with the switch connected to node A. Assume that all transistors have the transconductance $g_m = 1$ mA/V and neglect the effect of output resistance, please answer the following questions.
   (a) What feedback topology is adopted in the circuit (shunt-shunt, shunt-series, series-shunt, series-series)? [3 %].
   (b) Use the method of feedback analysis to find v_o/v_s. [7 %]
   (c) Determine the input resistance R_{in} which is defined as v_s/i_s? [3 %]

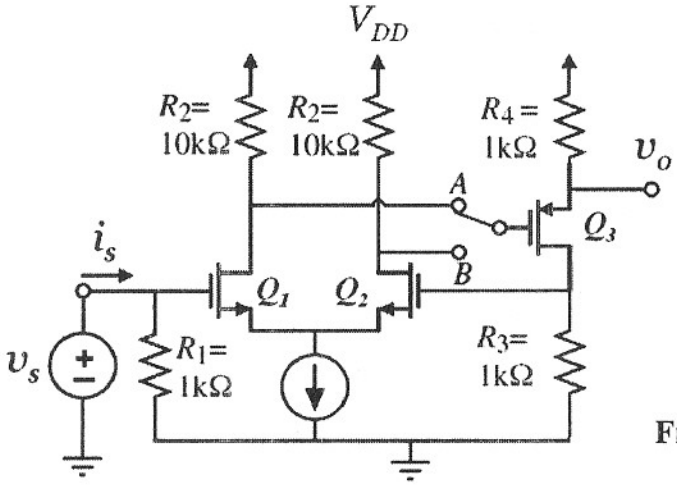

Figure 2

3. [12%] Shown in Figure 3 is the circuit cascading a source follower with common-gate amplifier. Let transconductance g_m = 5 mA/V, internal capacitances C_{gs} = 2 pF, internal capacitances C_{gd} = 0.1 pF, C_L = 1 pF, and R_{sig} = R_L = 20 KΩ. Neglect output resistance of the transistors and the body effect. Please answer the following questions.
   (a) Why does this configuration have excellent high-frequency performance? [3 %]
   (b) Why could this configuration solve the problem of low input resistance of the common-gate amplifier? [2 %]
   (c) Determine the frequencies of the poles [4 %], and 3-dB frequency f_H [3%].

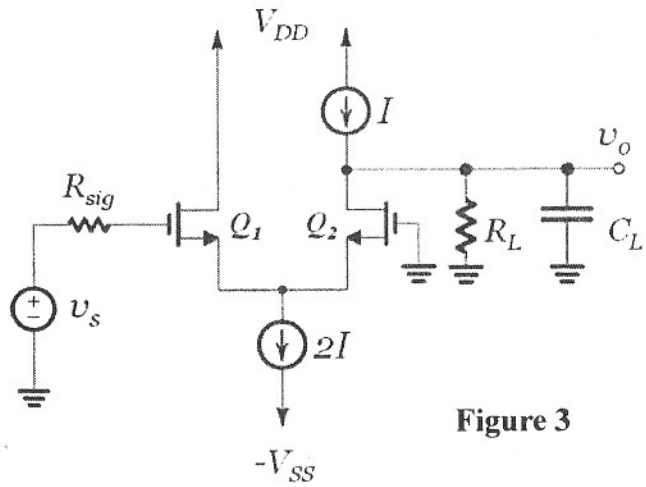

Figure 3

4. [15%] The MOSFET in the circuit of Figure 4 has V_t=1V, k_n W/L=1mA/V^2, and V_A=50V.
   (a) Find the values of R_S, R_D and R_G so that I_D=0.5mA, the largest possible value for R_D is used while a maximum signal swing at the drain of ±0.5V is possible, and the input resistance at the gate is 10MΩ. [3%]
   (b) If terminal Z is grounded, terminal X is connected to a signal source having a resistance of 5MΩ, and terminal Y is connected to a load resistance of 100KΩ, find the voltage gain from signal source to load. [4%]
   (c) If terminal Y is grounded, find the voltage gain from X to Z with Z open-circuited. What is the output resistance of the source follower? [4%]
   (d) If terminal X is grounded and terminal Z is connected to a current source delivering a signal current of 20μA and having a resistance of 200KΩ, find the voltage signal that can be measured at Y. For simplicity. (You may neglect the effect of r_o for this sub-question). [4%]

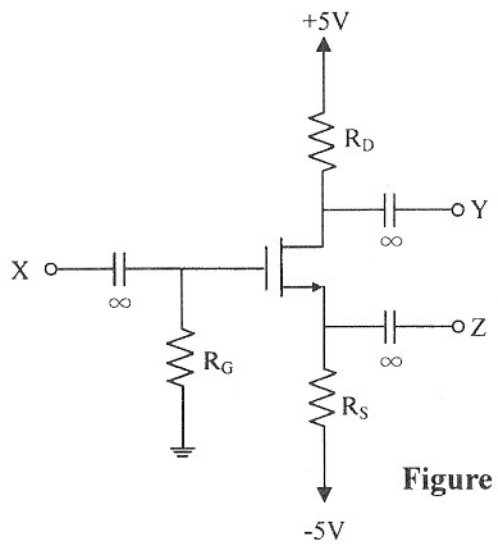

Figure 4

5. [10%] Assume that the SRAM cell (shown in Figure 5) is fabricated in a process technology for which $\mu_n C_{ox}=50\mu A/V^2$, $\mu_p C_{ox}=20\mu A/V^2$, $V_{tn0}=-V_{tp0}=1V$, $2\phi_f=0.6V$, $\gamma=0.5V^{1/2}$, and $V_{DD}=5V$. Let the Q1~Q4 have $(Width/Length=W/L)_n=4/2$, $(W/L)_p=10/2$, and let the Q5 and Q6 have (W/L)=10/2. Assuming that the SRAM cell is storing a 1 (Q=1) and that the capacitance of each bit line (BL, BLB) is 1pF. To simplify the analysis, assume that the BL and BLB are precharged to V_{DD}, and WL is GND at the initial condition.
   (a) What operation regions are Q1, Q3, Q5 and Q6 in (cutoff, saturation or triode) when WL is pulled up to V_{DD}? [4%]
   (b) Determine the time required to develop an output voltage of 0.2V on BLB when WL is pulled up to V_{DD}. [6%]

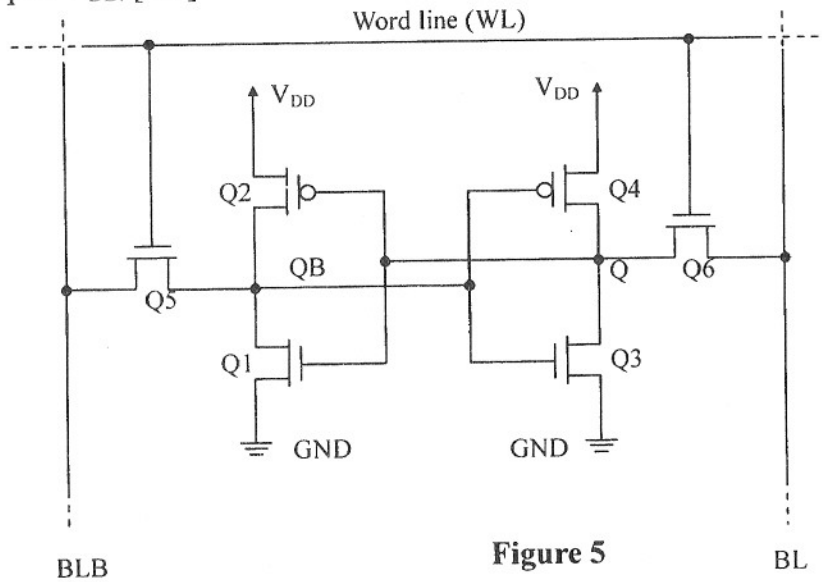

Figure 5

6. [15%] Design of the SR flip-flop.
   (a) Plot the schematic of a SR flip-flop realized by NAND gates. [5%]
   (b) List the truth table of the NAND flip-flop.[5%]
   (c) Sketch a circuit realization of the clocked NAND flip-flop.(Hint: clock signal as one of the input) [5%]

7. [10%] For the ring oscillator shown in Figure 6, assume $t_{pLH}=t_{pHL}$ for all gates.

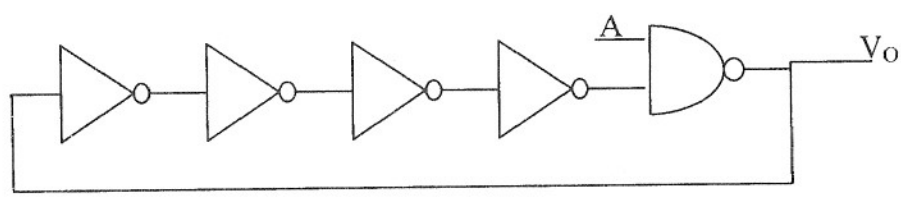

Figure 6

   (a) What should A be (logic 0 or 1) for the circuit to oscillate? [5%]
   (b) The oscillation frequency is found to be 2GHz. The delay time of the NAND gate and that of the inverters are identical, find the propagation delay, t_p, of the inverter. [5%]