國立清華大學 101 學年度碩士班考試入學試題

系所班組別：工業工程與工程管理學系

考試科目（代碼）：科技英文（1802）

1. Below was a news release from Intel, Samsung, and tsmc on their position for 450mm wafer manufacturing transition:

INTEL, SAMSUNG ELECTRONICS, TSMC REACH *AGREEMENT FOR 450mm WAFER MANUFACTURING* TRANSITION

Companies Target Common Timeline for 450mm Wafer Pilot Line Readiness

Issued by: INTEL, SAMSUNG ELECTRONICS and TSMC

Issued on: 2008/05/06

May 5, 2008 – Intel Corporation, Samsung Electronics and TSMC today announced they have reached agreement on the need for industry-wide collaboration to target a transition to larger, 450mm-sized wafers starting in 2012. The transition to larger wafers will enable continued growth of the semiconductor industry and helps maintain a reasonable cost structure for future integrated circuit manufacturing and applications.

The companies will cooperate with the semiconductor industry to help ensure that all of the required components, infrastructure and capability are developed and tested for a pilot line by this target date.

Historically, manufacturing with larger wafers helps increase the ability to produce semiconductors at a lower cost. The total silicon surface area of a 450mm wafer and the number of printed die (individual computer chips, for example) is more than twice that of a 300mm wafer. The bigger wafers help lower the production cost per chip. Additionally, through more efficient use of energy, water and other resources, bigger wafers can help diminish overall use of resources per chip. For example, the conversion from 200mm wafers to 300mm wafers helped reduce aggregate emissions per chip of air pollution, global warming gasses and water, and further reduction is expected with a transition to 450mm wafers.

"There is a long history of innovation and problem solving in our industry that has delivered wafer transitions resulting in lower costs per area of silicon processed and overall industry growth." said Bob Bruck, vice president and general manager, Technology Manufacturing Engineering in Intel's Technology and Manufacturing Group. "We, along with Samsung and TSMC, agree that the transition to 450mm

wafers will follow the same pattern of delivering increased value to our customers."

Intel, Samsung and TSMC indicate that the semiconductor industry can improve its return on investment and substantially reduce 450mm research and development costs by applying aligned standards, rationalizing changes from 300mm infrastructure and automation, and working toward a common timeline. The companies also agree that a cooperative approach will help minimize risk and transition costs.

"The transition to 450mm wafers will benefit the entire ecosystem of the IC industry, and Intel, Samsung, TSMC will work together with suppliers and other semiconductor manufacturers to actively develop 450mm capability," said Cheong-Woo Byun, senior vice president, Memory Manufacturing Operation Center, Samsung Electronics.

In the past, migration to the next larger wafer size traditionally began every 10 years after the last transition. For example, the industry began the transition to 300mm wafers in 2001, a decade after the initial 200mm manufacturing facilities (also known as "fabs") were introduced in 1991. Keeping in line with the historical pace of growth, Intel, Samsung and TSMC agree that 2012 is an appropriate target to begin the 450mm transition. Given the complexity of integrating all of the components for a transition of this size, the companies recognize that consistent evaluation of the target timeline will be critical to ensure industry-wide readiness.

"Increasing cost due to the complexity of advanced technology is a concern for the future," said Mark Liu, TSMC's senior vice president of Advanced Technology Business. "Intel, Samsung, and TSMC believe the transition to 450mm wafers is a potential solution to maintain a reasonable cost structure for the industry."

The three companies will continue to work with International Sematech (ISMI), as it plays a critical role in coordinating industry efforts on 450mm wafer supply, standards setting and developing equipment test bed capabilities.

Based on the above statement, **please list three reasons to support 450mm migration and each of the reasons should be less then 30 words** (21%).

2. In the *Guide for Authors* for paper submission, research Highlights are mandatory inputs as follows:

   Highlights are mandatory for this journal. They consist of a short collection of bullet points that convey the core findings of the article and should be submitted in a separate file in the online submission system. Please use 'Highlights' in the file name and include 3 to 5 bullet points (maximum 85 characters, including spaces, per bullet point). See http://www.elsevier.com/highlights for examples.

Please read below abstract of a journal paper and then try to extract **5 research highlights from the abstract** (**each highlight can use maximum 85 characters or 15 words**). (25%)

As semiconductor industry reached nano technology generation and consumer electronics era, the competition is no longer among individual semiconductor companies. Indeed, the collaborations among horizontally specialized value providers are critical for the success of the companies as well as the whole ecosystem. This paper aims to propose a novel index, i.e., Overall Wafer Effectiveness (OWE), to measure wafer productivity and drive various improvement directions for semiconductor ecosystem as a whole. Furthermore, the proposed OWE can be easily extended to incorporate additional attributes such as mask-field-utilization, throughput, and yield for effective management. We conducted a number of case studies in real settings. Indeed, an USA invention patent based on OWE has been granted and implemented. The results have shown that OWE can be employed as a semiconductor industry standard to drive collaborative efforts among IC designers, equipment vendors, and manufacturers in the ecosystem to enhance total wafer effectiveness. This paper concludes with discussions on value propositions of proposed OWE indices and future research directions.

3. **Please reorganize below paragraph and revise the sentences** to communicate the arguments in better logic and readability. (14%)

Driven by Moore's Law, the number of transistors fabricated in the same size area will be doubled every 12 to 24 months to provide more capability at equal or less cost, the semiconductor industry has strived for continuous technology migration and cost reduction. Semiconductor industry is very capital-intensive, in which the co-evolution of various semiconductor companies have been driven by technical advance and economical interest to maintain the growth and profitability via modularity and virtual integration. Semiconductor companies have coevolved in the ecosystem, in which the companies involved in various layers of semiconductor value chain work cooperatively and competitively to develop new technology, satisfy customer needs, and eventually incorporate the next round of innovations. Semiconductor industry is capital intensive, in which capacity utilization significantly affects the capital effectiveness and profitability of semiconductor companies. Thus, demand forecasting provides critical input to support strategic decisions of capacity planning and the associated capital expenditure that require long lead-time. Therefore, this study aims to predict the sales of semiconductor industry as a reference signal for individual companies to maintain a healthy ecosystem.

4. Please answer below questions. (25%)

[1]. Which one is "not" one of the properties of Just in Time (JIT)

(A). Customers receive their orders at the right time.

(B). A pull mode production system

(C). Stock level is based on economic order quantity (EOQ)

(D). Batch size is small

[2]. Which one is "not" one of the properties of Flexible Manufacturing System (FMS)

(A). A good method to achieve mass customization

(B). It need highly skilled labors

(C). It often has several different products being machined in FMS system

(D). The batch size of product should be fixed for line balancing

[3]. In supply chain management, vertical integration is a very important strategy to streamline the upstream suppliers and downstream buyers. Which one is "not" one of its benefits?

(A). Increase flexibility of supply chain network

(B). Lead to expansion of core competencies
(C). Increase entry barriers to potential competitors
(D). Capture upstream or downstream profit margins.

[4]. In opposition to vertical integration, horizontal integration strategy seeks to sell a type of product in numerous markets. Which one is "not" one of its benefits?
(A). Economies of scale
(B). Reduce competitors
(C). Improve supply chain coordination
(D). Increase market share

[5]. Concurrent Engineering (CE) is a systematic approach to the integrated, concurrent design of products and their related processes from conception to disposal during product design stage. Which one is not" one of the properties of CE?
(A). It can discover problem early
(B). It can reduce the product develop time
(C). It can minimize the horizontal overlap between the consecutive tasks
(D). It is a multi-disciplinary work

5. Please read below story and then answer the questions as detail as possible. (15%)

One winter a Farmer found a Snake stiff and frozen with cold. He had compassion on it, and taking it up, placed it in his bosom. The Snake was quickly revived by the warmth, and resuming its natural instincts, bit its benefactor, inflicting on him a mortal wound. "Oh," cried the Farmer with his last breath, "I am rightly served for pitying a scoundrel."

(A). Please point out three possible reasons why the farmer chose to save snake's life? (6%)

(B). What will happen if the snake didn't attack the farmer? Describe two possible consequences. (4%)

(C). In your opinion, what is the insight of this story? (5%)