

Demonstration of a High Speed 4-Channel Integrated Silicon Photonics WDM Link with Hybrid Silicon Lasers

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Abstract: The demonstration of a $4\lambda \times 10\text{Gbps}$ Silicon Photonics CWDM link integrating all optical components, electronics and packaging technologies required for system integration is reported. Further demonstration of the link operating at 50Gbps, $4\lambda \times 12.5\text{Gbps}$, is also shown.

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1. Introduction

The need for increased IO bandwidth in and around the CPU in many different computer systems has stimulated the research into optical interconnects for many years. Intel has been pursuing Silicon Photonics, a technology which creates optical components from a silicon substrate, as a candidate for these applications and has developed a series of silicon based photonic components [1- 3]. Here we report on a silicon photonics based WDM link demonstrating all the key technologies required to create a viable optical link for system integration. This 4-channel CWDM integrated silicon photonics link was designed to operate at a line rate of 10Gbps per channel; during the course of testing it was over-clocked to operate at 12.5Gbps per channel to demonstrate a 50Gbps aggregate bandwidth silicon photonics link.

2. Silicon Photonics Integrated Transmitter and Receiver

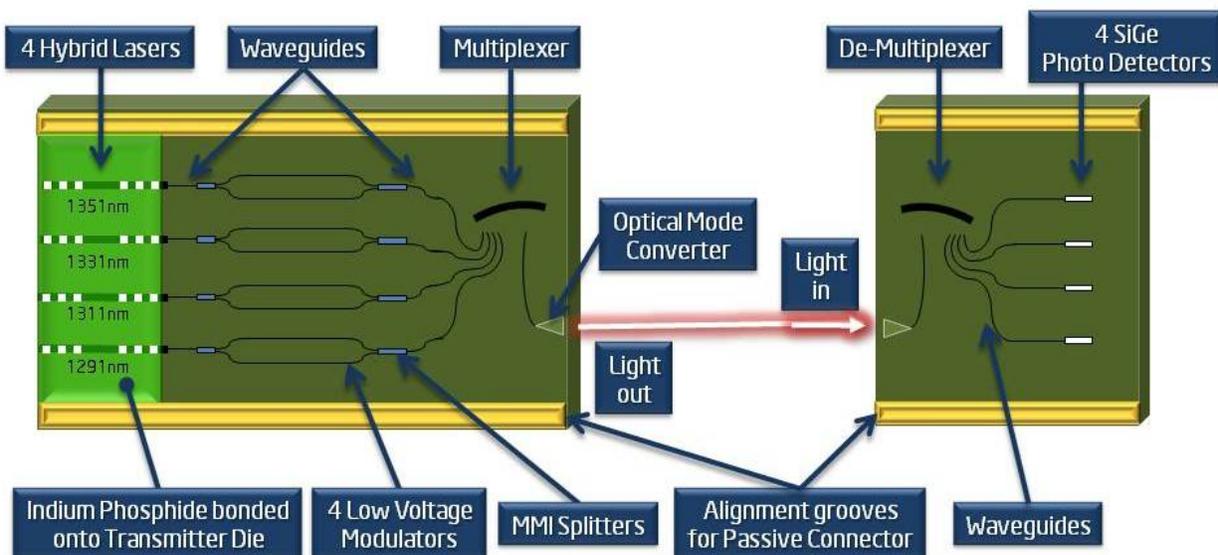


Figure 1. Schematics of the integrated 4-channel CWDM silicon photonics transmitter die (left) and receiver die (right)

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The hybrid silicon laser technology [1] was integrated for the first time onto the same substrate as a travelling wave optical modulator array [2], an Echelle grating based multiplexer and an inverted taper. The output power from the four hybrid silicon lasers, measured at the output of the integrated transmitter die, ranged from a minimum of 2mW for the lowest output power channel to 9mW for the highest power channels. The lasers were fabricated with a Distributed Bragg Reflector (DBR) in the silicon waveguide as the reflector and wavelength selection element. The modulators were driven by an approximately 1.35V peak-to-peak single-ended voltage provided by an Intel designed CMOS driver IC fabricated in the TSMC 65nm process. The driver and integrated transmitter were both flip chip mounted to an organic substrate, and the entire system was designed to operate at 10Gbps at room temperature with a passive heat sink. Optical coupling was based on passive alignment and relied upon high precision metal alignment pins seated into v-grooves in the silicon substrate to create alignment features for an external molded plastic lens assembly.

The transmitter demonstrated a phase efficiency of 3.3 V*cm, as predicted, a rise/fall time of 41 to 44ps, an extinction ratio ranging from 4.4dB to 6.3dB and a total jitter of 23 to 34ps.

The integrated receiver consisted of a de-multiplexer monolithically integrated with an array of high speed SiGe PIN photodetectors fabricated on a Silicon-on-Insulator (SOI) substrate, similar to previously published results [3]. Optical coupling between the receiver die and the optical fiber was based on the same passive optical alignment approach as was described above for the transmitter. The measured 3dB bandwidth of the four photodetectors was in the range of 9.4-10.6GHz when measured in a 50Ω system, with a measured responsivity of approximately 0.9A/W. The integrated receiver was flip chip attached to a separate organic substrate which was co-packaged with a commercially available 4-channel receiver IC.

3. System Performance

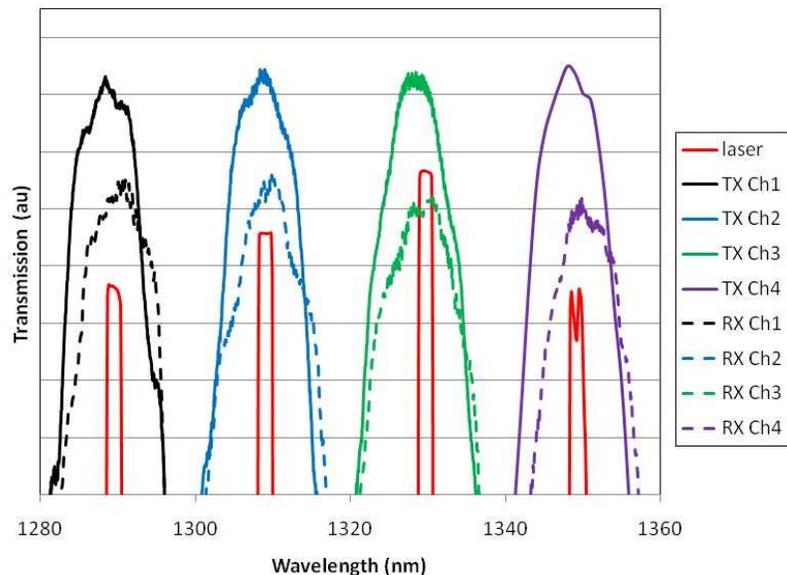


Figure 2. The wavelength channel alignment of the silicon hybrid laser, the Echelle grating multiplexer and the demultiplexer. Wavelength alignment was achieved to within 1nm between all components.

Achieving alignment of the wavelength channels between the hybrid silicon laser, the multiplexer and the demultiplexer without active cooling was a major design criteria for the system. The four wavelength channels were chosen to align with the ITU-T G.694.2 grid at 1291, 1311, 1331 and 1351nm. The alignment of the wavelength channels between the three components, with only passive heat sinking, is shown in Figure 2. The wavelength misalignment between the channel centers is within 1nm, and we estimate that the total link penalty due to this mismatch was <0.3dB.

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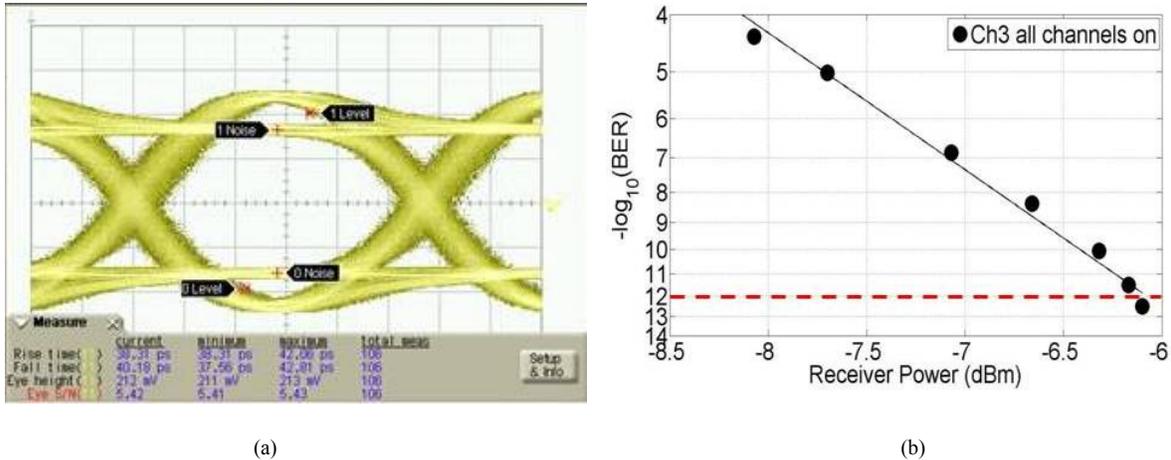


Figure 3a & b. (a) A 10Gbps eye diagram of a typical system link channel measured at the output of the receiver. (b) System BER versus received power for full 40Gbps link operation

Measurements from the eye diagram image shown in Figure 3a, which shows the output of the receiver for a typical wavelength channel during 10Gbps operation, show a rise and fall time of approximately 40ps. BER measurements as a function of average optical power at the input of the receiver chip were also taken, and typical results are shown in Figure 3b. The curve shown in Figure 3b demonstrates that a BER of $<10^{-12}$ was achieved with a received average optical power greater than -6.2dBm for this integrated link with all four channels running simultaneously. Separate measurements of the total link jitter performance showed a Total Jitter of ~ 45 ps, a Random Jitter component of ~ 2 ps and a Deterministic Jitter component of 17.5ps. The link was also characterized with all channels over-clocked to operate at 12.5Gbps; three of the four channels operated with $<10^{-12}$ BER, with the fourth demonstrating a BER of 3×10^{-10} .

4. Summary

The demonstration of a $4\lambda \times 10$ Gbps Silicon Photonics CWDM link integrating all optical components, electronics and packaging technologies required for system integration is reported. Results show a 40Gbps link operating with better than 10^{-12} BER with passive optical coupling on an organic substrate. Further demonstration of the link operating at 50Gbps, $4\lambda \times 12.5$ Gbps, is also discussed.

5. References

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6. Acknowledgements

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