中文摘要

在 IC 設計工業中，隨著技術越來越進步，設計也越來越複雜，經常會在設計的後端才發現問題，功能性的工程變更命令(ECO)的技術的應用，可有效的減少設計的時間以及製造的成本。在這篇論文，我們提出一個三階段的演算法，找尋兩電路最少的相異部分，最後利用邏輯閘回收使用的方法減少相異的部分。第一階段，從輸出端找尋結構等價的部分，第二階段，使用可滿足性(SAT)檢測程式，找尋兩電路邏輯等價的輸入端邊界，第三階段，替換部分邏輯閘找尋邏輯等價的輸出端。利用這三階段找到的相異電路再進行減小。從實驗解果可以得知，在大部分的案例都有不錯的結果。

Abstract

In the IC industry, chip design cycles are becoming more compressed, while designs themselves are growing in complexity. Functional specifications are often modified late in the design cycle, after placement and routing are complete. These trends necessitate efficient methods to handle late-stage engineering change orders (ECOs) to the functional specification, often in response to errors discovered after much of the implementation is finished. In this thesis, we propose a three-stage algorithm for generating a minimal logic difference between an original circuit and a modified circuit. Our method has three different stages and we perform them in order to produce a better patch. In the first phase, we search from the primary outputs to find structural equivalence between the original circuit and the modified circuit. In the second phase, we modify DeltaSyn[1] to use a SAT solver to identify logic equivalence near the input-side boundary of the changes. In the third phase, we create levels in each gate. According to levels, we check logically equivalent and choose replaced gates. After the three different stages, a gate-recycle[2] process performs the patch minimization in the final step. Encouraging experimental results are obtained by our method.