國 立 清 華 大 學 命 題 紙

1. The circuit shown in Figure 1 is to be designed to deliver 10 V dc to a 20-Ω load resistive load.
   (a) Assuming the diode to be ideal, and the input line voltage to be 120 V ac (rms) with a 60-Hz frequency, determine the required transformer turns ratio. (3%)
   (b) Select a suitable capacitor value if the ripple at the output is to be less than 5% of the output voltage. (3%)
   (c) Calculate the average diode current. (3%)
   (d) Determine the peak diode current. (3%)
   (e) Find the maximum allowed reverse-bias diode voltage. (3%)

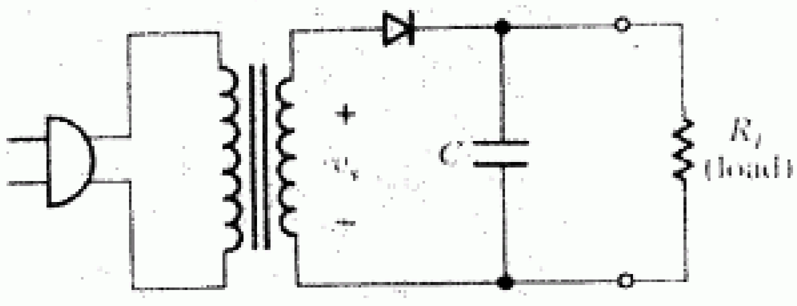

Figure 1

2. The basic circuit to be examined in the following two problems is shown in Figure 2(a). Possible amplifiers to be used in this circuit are given in Figure 2(b). For each of these circuits the drain and collector resistors can take on any values between 0 Ω and 20 Ω. In addition, you should consider that g_m = 2 mA/V (or 2 mS) for all FETs, and r_π = 1 kΩ and β = 100 for all BJT devices.
   (a) For the case where $R_{in} = 0$ and $R_L = \infty$, which of these circuits has the largest voltage gain (v_o/v_{in})? What is the value of this gain? (10%)
   (b) For the case where $R_{in} = 0$ and R_L = 1 kΩ, which of these circuits has the largest current gain (i_l/i_{in})? What is the value of this gain? (10%)

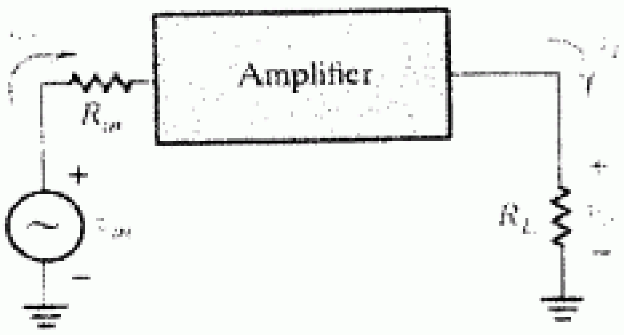

Figure 2(a)

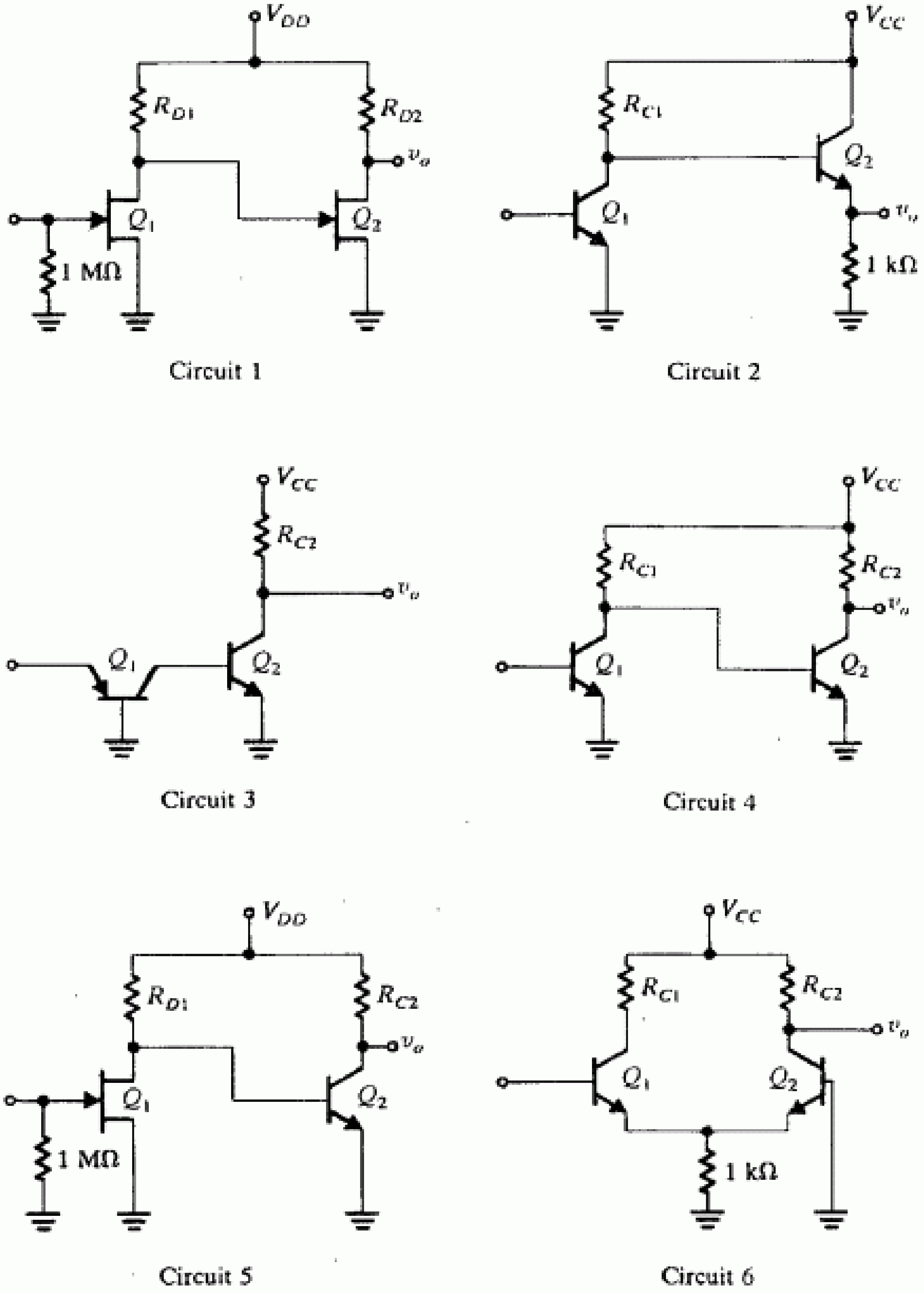
V_{DD}
R_{D1}
R_{D2}
v_o
Q_1
Q_2
1 MΩ
Circuit 1
V_{CC}
R_{C1}
Q_2
Q_1
v_o
1 kΩ
Circuit 2
V_{CC}
R_{C2}
v_o
Q_1
Q_2
Circuit 3
V_{CC}
R_{C1}
R_{C2}
v_o
Q_1
Q_2
Circuit 4
V_{DD}
R_{D1}
R_{C2}
v_o
Q_1
Q_2
1 MΩ
Circuit 5
V_{CC}
R_{C1}
R_{C2}
v_o
Q_1
Q_2
1 kΩ
Circuit 6

Figure 2(b)

3. (a) Calculate the small-signal gain of the circuit in Figure 3. Assume $\mu_n C_{ox}$ and V_t are the same for the two devices. Neglect channel-length modulation. (6%)

(b) If considering channel-length modulation, will the small-signal gain increase or reduce compared to the result obtained in (a)? Give a brief reason. (4%)

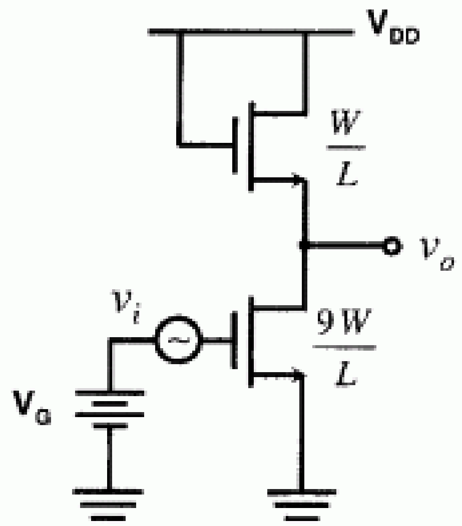

Figure 3

4. For the circuit in Figure 4,

(a) Derive I_{bias} (current flowing through M_1) in terms of R, $\mu_n C_{ox}$ and $(W/L)_n$, where $(W/L)_1 = 2(W/L)_n$, $(W/L)_2 = (W/L)_4 = (W/L)_5 = (W/L)_n$, $(W/L)_3 = 4(W/L)_n$, and $(W/L)_6 = (W/L)_7 = (W/L)_p$. Assume $|V_t|$ is the same for all devices. (10%)

(b) Derive the low-frequency small-signal gain (v_o/v_i). (7%)

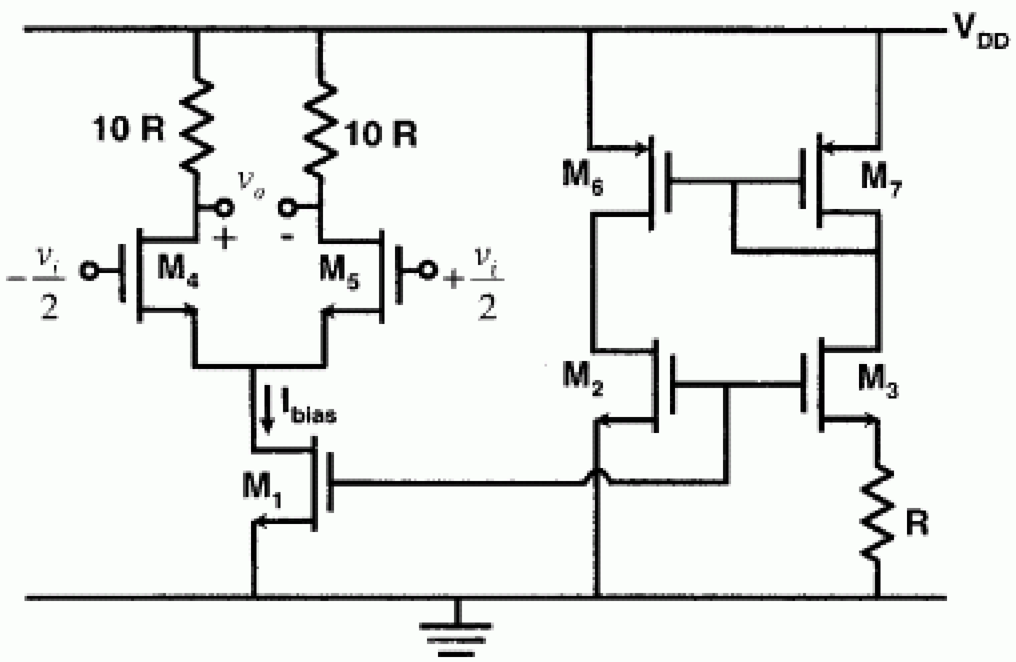

Figure 4

5. Circle the advantages of using emitter degeneration in an emitter-coupled differential pair (multiple choices): (4%)

(a) Higher gain

(b) Higher bandwidth

(c) Lower CMRR

(d) Increased linearity

6. Circle the correct descriptions for applying negative feedback to amplifiers (multiple choices): (4%)

(a) Reduce nonlinear distortion

(b) Gain becomes less sensitive to component variation

(c) Current amplifiers use series-shunt configuration

(d) Both input and output resistances reduce for a transresistance amplifier

7. The schematic of an multivibrator consist of a integrator (Op Amp 1) cascading with a non-inverting bistable circuitis (Op Amp 2) and the output waveform are shown in Figure 5. Assume the initial charge on C, $Q_C(t=0)=0$.

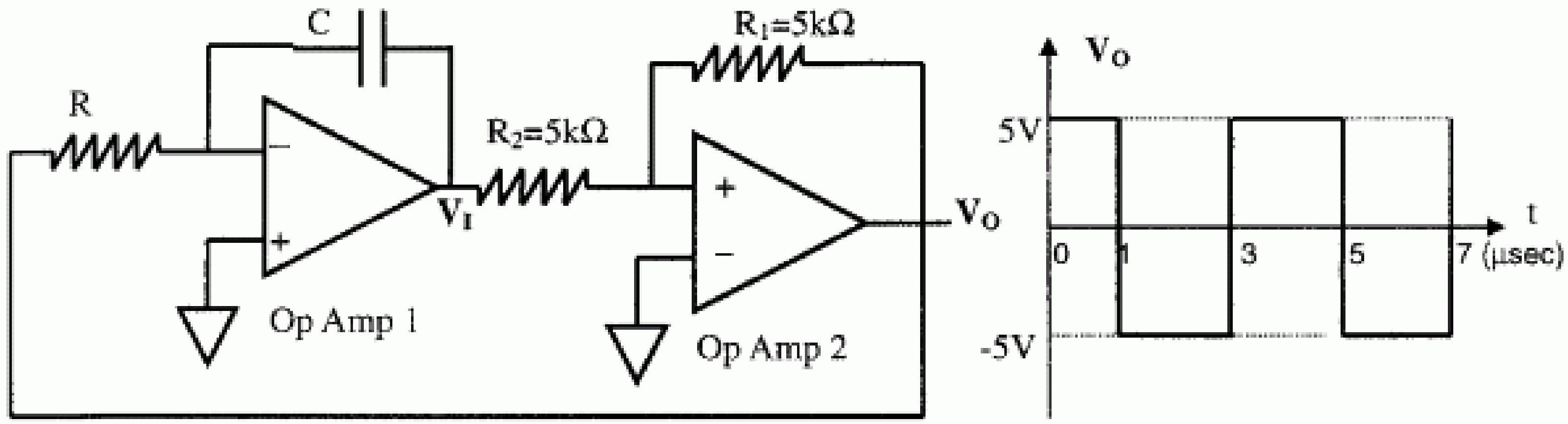

Figure 5

(a) R=1 kΩ , what is the value of C? (5%)

(b) Plot $V_I(t)$ from 0 to 7μsec. Please label clearly the slopes (dV_I/dt) and peak values of the waveform. (10%)

8. Let $Y = \overline{A} \cdot \overline{B} + \overline{C}$, assume only A, B, C inputs are available.

(a) Sketch a circuit implementation of Y by complementary CMOS logic circuits. (5%)

(b) Sketch a circuit implementation of Y by dynamic (clocked) logic circuits. (5%)

(c) Discuss the advantages and disadvantages of the logic gates in (a) and (b). (5%)