1 nm equivalent oxide thickness in $Ga_2O_3(Gd_2O_3)/In_{0.2}Ga_{0.8}As$ metal-oxide-semiconductor capacitors

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An equivalent oxide thickness about 1 nm for $Ga_2O_3(Gd_2O_3)$ (GGO) on $In_{0.2}Ga_{0.8}As$ has been achieved by employing a thin *in situ* deposited 3 nm thick Al_2O_3 protection layer. The dual gate oxide stacks of the Al_2O_3/GGO (33, 20, 10, 8.5, and 4.5 nm)/$In_{0.2}Ga_{0.8}As$/GaAs metal-oxide-semiconductor (MOS) capacitors remain amorphous after rapid thermal annealing up to 800–850 °C, accompanied with atomically sharp smooth oxide/semiconductor interfaces. Well behaved capacitance-voltage (*C-V*) curves of the MOS diodes have shown sharp transition from depletion to accumulation with small flatband voltage (1.1 V for Au metal gate and 0.1 V for Al), and weak frequency dispersion (1.5%–5.4%) between 10 and 500 kHz at accumulation capacitance. Low leakage current densities [3.1×10^{-5} and 2.5×10^{-9} A/cm^2 at $V=V_{fb}+1$ V for Al_2O_3(3 nm)/GGO(4.5 and 8.5 nm)], a high dielectric constant around 14–16 of GGO for all tested thicknesses, and a low interfacial density of states (D_{it}) in the low 10^{11} cm^{-2} eV^{-1} have also been accomplished. © *2008 American Institute of Physics*. [DOI: 10.1063/1.2918835]

Scaling high-κ oxides to nanometer range as well as unpinning surface Fermi level of the III-V semiconductors has been one main focus of recent high-κ research on high mobility channel materials.[1–3] Previously, we discovered that $Ga_2O_3(Gd_2O_3)$ (GGO) ultrahigh vacuum (UHV) deposited on III-V's of GaAs and InGaAs has unpinned surface Fermi level and showed low interfacial state density.[4,5] Inversion-channel and depletion-mode metal-oxide semiconductor field-effect transistors (MOSFETs) employing GGO as the gate dielectric were demonstrated.[6–8] Due to the tendency of GGO to absorb moisture upon air exposure leading to degradations of electrical performance,[9] relatively thick oxides in the range 25–55 nm were used in the earlier studies of MOS capacitors and transistors to minimize the moisture-absorption effects. Postannealing under UHV or flowing nitrogen gas of thick air-exposed GGO was shown to expel moisture, thus restoring low interfacial density of states (D_{it}) and low leakage currents, and maintaining smooth oxide-semiconductor interfaces.[10,11] However, very little work has been reported on scaling of equivalent oxide thickness (EOT) of GGO to 1 nm due to degraded oxide/III-V interfaces caused by air exposure, which may not be recovered upon UHV annealing, in contrast to thicker GGO films. Here, EOT is defined as $\kappa_{SiO_2}\times t_{high\ \kappa}/\kappa_{high\ \kappa}$.

In this letter, we demonstrate the GGO scaling approaching 1 nm EOT in GGO/$In_{0.2}Ga_{0.8}As$ (InGaAs) gate stack with the aid of an *in situ* deposited 3 nm thick Al_2O_3 on top of GGO, which serves as a protection layer owing to its thermal and chemical stabilities against moisture. MOS capacitors with the dual-dielectric layer on InGaAs were also shown to withstand rapid thermal annealing (RTA) to 800–850 °C. Excellent capacitance-voltage (*C-V*) characteristics in terms of small flatband voltage, a small frequency dispersion of measured capacitances at accumulation, and D_{it}'s in the low 10^{11} cm^{-2} eV^{-1} have been achieved. Moreover, the κ values of GGO remaining around 14–16 are obtained for all GGO thicknesses ranging from 33, 20, 10, and 8.5 nm to 4.5 nm (with κ values of 3 nm Al_2O_3 estimated to be 9–7). The smallest EOT of GGO achieved in this work is 1.25–1.1 nm, along with low leakage current densities of 3.1×10^{-5} and 2.5×10^{-9} A/cm^2 at biasing voltage of $V_{fb}+1$ V for GGO films of 4.5 and 8.5 nm, respectively.

Al_2O_3/GGO/InGaAs/GaAs MOS capacitor structures were grown in a multichamber UHV system,[4] which consists of a solid-source GaAs-based III-V molecular beam epitaxy chamber, two UHV oxide deposition chambers, and UHV wafer transfer modules. After growth of an *n*-type 7.5 nm thick $In_{0.2}Ga_{0.8}As$ (Si doping of 4×10^{17}/cm^3) and an *n*-type 225 nm thick GaAs epilayer (Si doping of 4×10^{17}/cm^3) on N^+ GaAs substrates, the wafers were transferred *in situ* to the oxide chambers for depositing GGO and Al_2O_3 in sequence. Si_3N_4 was deposited on the back side of the wafer to prevent preferential arsenic evaporation during the *ex situ* RTA. Au or Al was used as the gate metal. E-beam deposited AuGe/Ni/Au was used as the back side Ohmic electrical contacts after Si_3N_4 layers were etched off.[12]

Systematic RTAs to 800 and 850 °C were applied to the oxide stacks, as the high-temperature annealing is important for dopant activation[13] in fabricating inversion-channel MOSFETs. *C-V* and *J-E* characteristics were measured using Agilent 4284 and 4156C, respectively, where *J* is the leakage current density as *I* divided by the Au or Al electrode area, and *E* is the electrical field as *V* divided by the total thickness of the dual oxide stack. High-resolution transmission electron microscopy (HRTEM) was used to examine the interfacial roughness, oxide thickness, and integrity of the MOS structures. D_{it} near the midgap was deduced using the high frequency conductance method.[14]

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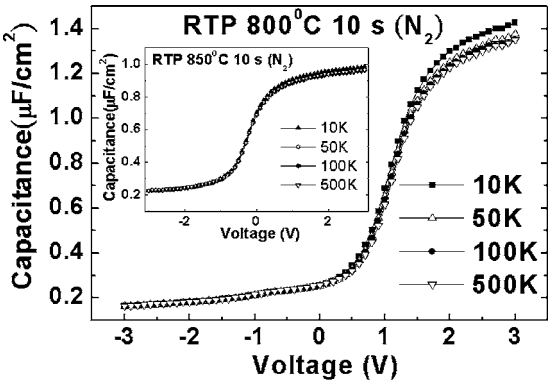

FIG. 1. *C-V* characteristics for an Al_2O_3(3 nm)/GGO(4.5 nm)/$In_{0.2}Ga_{0.8}As$/GaAs MOS diode RTA to 800 °C with the Au gate deposited afterwards. The inset shows *C-V* characteristics of another 8.5 nm sample, which was RTA to 850 °C with the Al gate. The capacitor area is 7.85×10^{-5} cm^2.

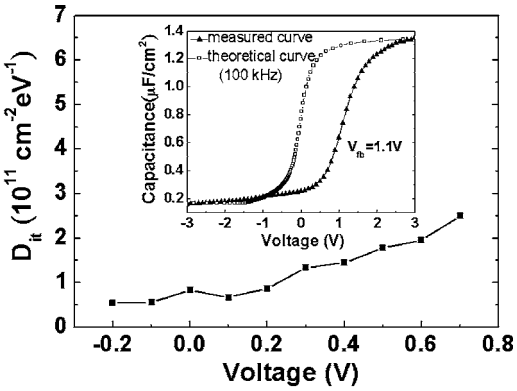

FIG. 2. Distribution of D_{it} (4.5 nm sample of Fig. 1) near the midgap measured using the high frequency conductance method. Small flatband voltage and differences between the measured and theoretical *C-V* curve at 100 kHz are shown in the inset.

C-V curves for all tested samples exhibit a clear transition from accumulation, depletion, to inversion under various frequencies, indicating an unpinned surface Fermi level at the GGO/InGaAs interface. The *C-V* curves of a 4.5 nm sample are given in Fig. 1, with inset showing the 8.5 nm sample data. The results also illustrate a vital role of Al_2O_3 in the dual-dielectric stacks for encapsulating the dielectrics to eliminate/reduce the moisture absorption in GGO. This has effectively passivated $In_{0.2}Ga_{0.8}As$ as GGO's EOT being scaled down to around 1 nm. Moreover, unlike the previous report that the bulk and interfacial properties of the oxide/III-V's degraded after RTA over 800 °C due to interdiffusions between atomic layer deposition (ALD) grown Al_2O_3 and GaAs (or InGaAs),[2] the sharp transition from accumulation and depletion in our *C-V* data indicates the robustness of the Al_2O_3/GGO gate stacks and the dielectrics/InGaAs heterostructures after RTA. We attribute this result to the absence of In_2O_3 and Ga_2O_3 near the interface by our UHV oxide deposition, whereas such residual native oxides were observed in the ALD approach.[15]

The dielectric constant (κ) for GGO of all tested thicknesses is around 14–16, deduced from the measured accumulation capacitance C_{max}, the capacitor area, and the oxide thickness, by using the series capacitor equation[16] with a κ value for Al_2O_3 assumed to be around 7–9. Figure 1 also shows a small frequency dispersion of ~5% at C_{max} in the frequency range from 10 to 500 kHz, again indicating small amounts of interfacial traps between high-κ GGO and $In_{0.2}Ga_{0.8}As$. Detailed electrical properties for all of the samples are listed in Table I. The measured capacitance dispersion as small as 1.5% may be the smallest among all work reported for high-κ dielectrics on the III-V's.

By measuring peak values of equivalent parallel conductance versus frequency required by the high frequency conductance method,[14,16] the dependence of D_{it} as a function of the applied voltage was shown in Fig. 2 for the 4.5 nm sample. The D_{it} near the midgap was deduced to be about 1.3×10^{11} cm^{-2} eV^{-1}. From the distribution of D_{it} around the midgap, all D_{it} values lie in the low 10^{11} cm^{-2} eV^{-1}, implying excellent thermal stability of the Al_2O_3/GGO/InGaAs withstanding RTA to 800 °C. The small difference between the measured and theoretical *C-V* curves at 100 kHz in the inset of Fig. 2 gives a flatband voltage (V_{fb}) of 1.1 V, consistent with the theoretically predicted flatband voltage V_{fb} around 1.1 V, as utilizing 5.3–5.4 eV for the work function of Au and 4.24 eV for the work function of highly doped $In_{0.2}Ga_{0.8}As$. The small flatband voltage illustrates the effectiveness of 800 °C annealing to greatly reduce bulk electrically active traps, which may have been accumulated during the e-beam deposition of Al_2O_3/GGO.

The *J-E* measurements have been performed on all of the tested samples RTA to 800–850 °C, as listed in Table I.

TABLE I. Summary of GGO scalability and relevant electrical properties, including GGO dielectric constant (κ), flatband voltage (V_{fb}), frequency dispersion of capacitance at accumulation, leakage current density at $V_g = V_{fb} + 1$ V, interfacial density of states (D_{it}) near the midgap, and GGO EOT values.

GGO thickness (nm)	GGO κ value	V_{fb} (V)	Dispersion (10–500 kHz) (%)	$J@V_{fb}+1$ V (A/cm^2)	D_{it} (10^{11} cm^{-2} eV^{-1})	GGO EOT (nm)
Au gate metal (RTA 800 °C 10 s)						
33	15–16	3.5	2.8	1.18×10^{-9}	1.3	8.6–8.0
20	14–15	1.3	1.5	1.62×10^{-9}	1	5.6–5.2
10	14–15	1.1	2.2	1.46×10^{-9}	1.4	2.8–2.6
8.5	14–16	1.1	4.7	1.78×10^{-9}	2.6	2.4–2.1
4.5	14–16	1.1	5.4	3.1×10^{-5}	1.3	1.3–1.1
Al gate metal (RTA 850 °C 10 s)						
8.5	14–16	0.1	2.6	2.5×10^{-9}	2.5	2.4–2.1

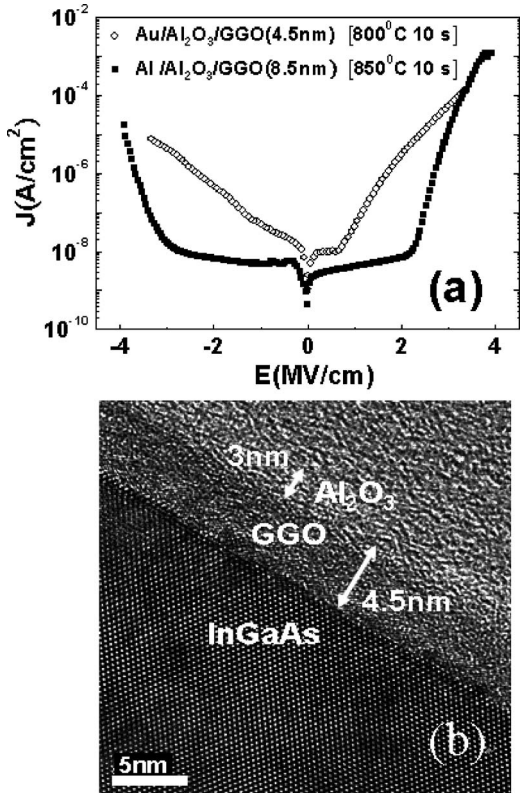

FIG. 3. (a) Leakage current density (J) for 4.5 and 8.5 nm samples, subjected to RTA 800 °C 10 s, and 850 °C 10 s under N_2, respectively. (b) Cross-sectional HRTEM image of the 4.5 nm sample in (a).

Figure 3(a) exhibits leakage current densities of 3.1×10^{-5} and 2.5×10^{-9} A/cm^2 at $V_g=V_{fb}+1$ V for the 4.5 and 8.5 nm GGOs, respectively. The low electrical leakage demonstrates the excellent thermodynamic stability, the high quality, and integrity of Al_2O_3/GGO dual oxide after air exposure and post-high-temperature annealing (800–850 °C).

Figure 3(b) shows the HRTEM image of the thinnest sample, indicating an atomically sharp, smooth oxide/semiconductor interface, oxide thermal stability, and average oxide thickness of 4.5 nm. A sharp transition from crystalline InGaAs to GGO was observed, and GGO and Al_2O_3 remain amorphous, even after air exposure and high-temperature annealing. The results indicate that GGO, as thin as ~1 nm EOT, is highly thermodynamically stable as long as it is moisture-free, similar to or even better than our previous results on thicker oxides (≥20 nm).[10,11] HRTEM studies on the 8.5 nm sample after RTA to 850 °C also showed similar behavior (not shown).

When $Ga_2O_3(Gd_2O_3)$ was thinner than 10 nm and without protection, we have previously found that its dielectric constant is much less than the value measured in the films thicker than 20 nm. For example, a κ value of 9 was obtained for 5.7 nm GGO deposited on GaAs, despite the application of an UHV annealing. *Ex situ* deposited ~2–3 nm thick Si_3N_4 as a cap on 7–8 nm thick GGO has led to a working inversion-channel InGaAs MOSFET,[3] yet the EOT of GGO remained as high as 4 nm.

In conclusion, our results unambiguously demonstrated the attainment of high-quality bulk and interfacial properties of $Al_2O_3/Ga_2O_3(Gd_2O_3)/In_{0.2}Ga_{0.8}As/GaAs$ after a stringent test of RTA up to 800–850 °C, one common way for fabricating inversion-channel MOSFETs. The achieved excellent electrical characteristics after the high-temperature RTA are even superior to our previous results of thicker $Ga_2O_3(Gd_2O_3)$, and are among the best in the high-κ/III-V systems. Furthermore, $Ga_2O_3(Gd_2O_3)$ remains amorphous withstanding annealing to 850 °C as well as maintaining atomically smooth interfaces with InGaAs. Hence, the *in situ* Al_2O_3 cap plays a vital role in extending our earlier success of unpinning surface Fermi level in the III-V's to an aggressive scaling $Ga_2O_3(Gd_2O_3)$ down to ~1 nm EOT, enhancing the prospect for realistic device applications. Future work includes further thinning of the *in situ* Al_2O_3 capping layer and/or *in situ* deposition of metal gates.

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