Scaling high-κ oxides to nanometer range as well as unpinning surface Fermi level of the III-V semiconductors has been one main focus of recent high-κ research on high mobility channel materials.1–3 Previously, we discovered that Ga2O3(Gd2O3) (GGO) ultrahigh vacuum (UHV) deposited on III-V’s of GaAs and InGaAs has unpinned surface Fermi level and showed low interfacial state density.4,5 Inversion-channel and depletion-mode metal-oxide semiconductor field-effect transistors (MOSFETs) employing GGO as the gate dielectric were demonstrated.6–8 Due to the tendency of GGO to absorb moisture upon exposure leading to degradation of electrical performance,9 relatively thick oxides in the range 25–55 nm were used in the earlier studies of MOS capacitors and transistors to minimize the moisture sensitivity of the high dielectric constant around 14–16 of GGO for all tested thicknesses, and a low interfacial density of states (Dn) in the low 1011 cm−2 eV−1 have also been accomplished. © 2008 American Institute of Physics. [DOI: 10.1063/1.2918835]

1 nm equivalent oxide thickness in Ga2O3(Gd2O3)/In0.2Ga0.8As metal-oxide-semiconductor capacitors

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An equivalent oxide thickness about 1 nm for Ga2O3(Gd2O3) (GGO) on In0.2Ga0.8As has been achieved by employing a thin in situ deposited 3 nm thick Al2O3 protection layer. The dual gate oxide stacks of the Al2O3/GGO (33, 20, 10, 8.5, and 4.5 nm)/In0.2Ga0.8As/GaAs metal-oxide-semiconductor (MOS) capacitors remain amorphous after rapid thermal annealing up to 800–850 °C, accompanied with atomically sharp smooth oxide-semiconductor interfaces. Well behaved capacitance-voltage (C-V) curves of the MOS diodes have shown sharp transition from depletion to accumulation with small flatband voltage (1.1 V for Au metal gate and 0.1 V for Al), and weak frequency dispersion (1.5%–5.4%) between 10 and 500 kHz at accumulation capacitance. Low leakage current densities [3.1 × 10−5 and 2.5 × 10−9 A/cm2 at V = Vfb + 1 V for Al2O3(3 nm)/GGO(4.5 and 8.5 nm)], a high dielectric constant around 14–16 of GGO for all tested thicknesses, and a low interfacial density of states (Dn) in the low 1011 cm−2 eV−1 have also been accomplished.© 2008 American Institute of Physics.

Scaling high-κ oxides to nanometer range as well as unpinning surface Fermi level of the III-V semiconductors has been one main focus of recent high-κ research on high mobility channel materials.1–3 Previously, we discovered that Ga2O3(Gd2O3) (GGO) ultrahigh vacuum (UHV) deposited on III-V’s of GaAs and InGaAs has unpinned surface Fermi level and showed low interfacial state density.4,5 Inversion-channel and depletion-mode metal-oxide semiconductor field-effect transistors (MOSFETs) employing GGO as the gate dielectric were demonstrated.6–8 Due to the tendency of GGO to absorb moisture upon exposure leading to degradation of electrical performance,9 relatively thick oxides in the range 25–55 nm were used in the earlier studies of MOS capacitors and transistors to minimize the moisture-sensitivity effects. Postannealing under UHV or flowing nitrogen gas of thick air-exposed GGO was shown to expel moisture, thus restoring low interfacial density of states (Dn) and low leakage currents, and maintaining smooth oxide-semiconductor interfaces.10,11 However, very little work has been reported on scaling of equivalent oxide thickness (EOT) of GGO to 1 nm due to degraded oxide/III-V interfaces caused by air exposure, which may not be recovered upon UHV annealing, in contrast to thicker GGO films. Here, EOT is defined as κSiO2 × h/n κhigh × κhigh κ.

In this letter, we demonstrate the GGO scaling approach-1 1 nm EOT in GGO/In0.2Ga0.8As (InGaAs) gate stack with the aid of an in situ deposited 3 nm thick Al2O3 on top of GGO, which serves as a protection layer owing to its thermal and chemical stabilities against moisture. MOS capacitors with the dual-dielectric layer on InGaAs were also shown to withstand rapid thermal annealing (RTA) to 800–850 °C. Excellent capacitance-voltage (C-V) characteristics in terms of small flatband voltage, a small frequency dispersion of measured capacitances at accumulation, and Dn’s in the low 1011 cm−2 eV−1 have been achieved. Moreover, the κ values of GGO remaining around 14–16 are obtained for all GGO thicknesses ranging from 33, 20, 10, and 8.5 nm to 4.5 nm (with κ values of 3 nm Al2O3 estimated to be 9–7). The smallest EOT of GGO achieved in this work is 1.25–1.1 nm, along with low leakage current densities of 3.1 × 10−5 and 2.5 × 10−9 A/cm2 at biasing voltage of Vfb + 1 V for GGO films of 4.5 and 8.5 nm, respectively.

Al2O3/GGO/InGaAs/GaAs MOS capacitor structures were grown in a multichamber UHV system,4 which consists of a solid-source GaAs-based III-V molecular beam epitaxy chamber, two UHV oxide deposition chambers, and UHV wafer transfer modules. After growth of an n-type 7.5 nm thick In0.2Ga0.8As (Si doping of 4 × 1017/cm3) and an n-type 225 nm thick GaAs epilayer (Si doping of 4 × 1017/cm3) on N+ GaAs substrates, the wafers were transferred in situ to the oxide chambers for depositing GGO and Al2O3 in sequence. Si3N4 was deposited on the back side of the wafer to prevent preferential arsenic evaporation during the ex situ RTA. Au or Al was used as the gate metal. E-beam deposited AuGe/Ni/Au was used as the back side Ohmic electrical contacts after Si3N4 layers were etched off.12

Systematic RTAs to 800 and 850 °C were applied to the oxide stacks, as the high-temperature annealing is important for dopant activation13 in fabricating inversion-channel MOSFETs. C-V and J-E characteristics were measured using Agilent 4284 and 4156C, respectively, where J is the leakage current density as I divided by the Au or Al electrode area, and E is the electrical field as V divided by the total thickness of the dual oxide stack. High-resolution transmission electron microscopy (HRTEM) was used to examine the interfacial roughness, oxide thickness, and integrity of the MOS structures. Dn near the midgap was deduced using the high frequency conductance method.14

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C-V curves for all tested samples exhibit a clear transition from accumulation, depletion, to inversion under various frequencies, indicating an unpinned surface Fermi level at the GGO/InGaAs interface. The C-V curves of a 4.5 nm sample are given in Fig. 1, with inset showing the 8.5 nm sample data. The results also illustrate a vital role of Al$_2$O$_3$ in the dual-dielectric stacks for encapsulating the dielectrics to eliminate/reduce the moisture absorption in GGO. This has effectively passivated In$_{0.2}$Ga$_{0.8}$As as GGO's EOT being scaled down to around 1 nm. Moreover, unlike the previous report that the bulk and interfacial properties of the oxide/III-V's degraded after RTA over 800 °C due to interdiffusions between atomic layer deposition (ALD) grown Al$_2$O$_3$ and GaAs (or InGaAs), the sharp transition from accumulation and depletion in our C-V data indicates the robustness of the Al$_2$O$_3$/GGO gate stacks and the dielectrics/InGaAs heterostructures after RTA. We attribute this result to the absence of In$_2$O$_3$ and Ga$_2$O$_3$ near the interface by our UHV e-beam deposition of Al$_2$O$_3$.

The dielectric constant ($\kappa$) for GGO of all tested thicknesses is around 14–16, deduced from the measured capacitance $C_{\text{max}}$, the capacitor area, and the oxide thickness, by using the series capacitor equation with a $\kappa$ value for Al$_2$O$_3$ assumed to be around 9. Figure 1 also shows a small frequency dispersion of ~5% in the frequency range from 10 to 500 kHz, again indicating small amounts of interfacial traps between high-\(\kappa\) GGO and In$_{0.2}$Ga$_{0.8}$As. Detailed electrical properties for all of the samples are listed in Table I. The measured capacitance dispersion as small as 1.5% may be the smallest among all work reported for high-\(\kappa\) dielectrics on the III-V's.

By measuring peak values of equivalent parallel conductance versus frequency required by the high frequency conductance method, the dependence of $D_h$ as a function of the applied voltage was shown in Fig. 2 for the 4.5 nm sample. The $D_h$ near the midgap was deduced to be about $1.3 \times 10^{11}$ cm$^-2$ eV$^-1$. From the distribution of $D_h$ around the midgap, all $D_h$ values lie in the low $10^{11}$ cm$^-2$ eV$^-1$, implying excellent thermal stability of the Al$_2$O$_3$/GGO/InGaAs withstanding RTA to 800 °C. The small difference between the measured and theoretical C-V curves at 100 kHz in the inset of Fig. 2 gives a flatband voltage $V_{fb}$ of 1.1 V, consistent with the theoretically predicted flatband voltage $V_{fb}$ of 1.1 V, as utilizing 5.3–5.4 eV for the work function of Au and 4.24 eV for the work function of highly doped In$_{0.2}$Ga$_{0.8}$As. The small flatband voltage illustrates the effectiveness of 800 °C annealing to greatly reduce bulk electrically active traps, which may have been accumulated during the e-beam deposition of Al$_2$O$_3$/GGO.

The J-E measurements have been performed on all of the tested samples RTA to 800–850 °C, as listed in Table I.

![Image](https://www.aip.org/content/aip/journal/apl/92/17/10.1063/1.3000699)  
RTP 800 °C 10 s (N$_p$)

**TABLE I.** Summary of GGO scalability and relevant electrical properties, including GGO dielectric constant ($\kappa$), flatband voltage ($V_{fb}$), frequency dispersion of capacitance at accumulation, leakage current density at $V=V_{fb}+1$ V, interfacial density of states ($D_h$) near the midgap, and GGO EOT values.

<table>
<thead>
<tr>
<th>GGO thickness (nm)</th>
<th>GGO $\kappa$ value</th>
<th>$V_{fb}$ (V)</th>
<th>Dispersion (10–500 kHz) (%)</th>
<th>$J@V_{fb}+1$ V (A/cm$^2$)</th>
<th>$D_h$ ($10^{11}$ cm$^-2$ eV$^-1$)</th>
<th>GGO EOT (nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>33</td>
<td>15–16</td>
<td>3.5</td>
<td>2.8</td>
<td>$1.18 \times 10^{-9}$</td>
<td>1.3</td>
<td>8.6–8.0</td>
</tr>
<tr>
<td>20</td>
<td>14–15</td>
<td>1.3</td>
<td>1.5</td>
<td>$1.62 \times 10^{-9}$</td>
<td>1</td>
<td>5.6–5.2</td>
</tr>
<tr>
<td>10</td>
<td>14–15</td>
<td>1.1</td>
<td>2.2</td>
<td>$1.46 \times 10^{-9}$</td>
<td>1.4</td>
<td>2.8–2.6</td>
</tr>
<tr>
<td>8.5</td>
<td>14–16</td>
<td>1.1</td>
<td>4.7</td>
<td>$1.78 \times 10^{-9}$</td>
<td>2.6</td>
<td>2.4–2.1</td>
</tr>
<tr>
<td>4.5</td>
<td>14–16</td>
<td>1.1</td>
<td>5.4</td>
<td>$3.1 \times 10^{-5}$</td>
<td>1.3</td>
<td>1.3–1.1</td>
</tr>
</tbody>
</table>

Al gate metal (RTA 850 °C 10 s)

<table>
<thead>
<tr>
<th>GGO thickness (nm)</th>
<th>GGO $\kappa$ value</th>
<th>$V_{fb}$ (V)</th>
<th>Dispersion (10–500 kHz) (%)</th>
<th>$J@V_{fb}+1$ V (A/cm$^2$)</th>
<th>$D_h$ ($10^{11}$ cm$^-2$ eV$^-1$)</th>
<th>GGO EOT (nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>8.5</td>
<td>14–16</td>
<td>0.1</td>
<td>2.6</td>
<td>$2.5 \times 10^{-9}$</td>
<td>2.5</td>
<td>2.4–2.1</td>
</tr>
</tbody>
</table>

![Image](https://www.aip.org/content/aip/journal/apl/92/17/10.1063/1.3000699)  
Distribution of $D_h$ (4.5 nm sample of Fig. 1) near the midgap measured using the high frequency conductance method. Small flatband voltage and differences between the measured and theoretical C-V curve at 100 kHz are shown in the inset.
results on thicker oxides moisture-free, similar to or even better than our previous EOT, is highly thermodynamically stable as long as it is annealing. The results indicate that GGO, as thin as 8.5 nm sample after RTA to 850 °C also showed similar integrity of Al2O3 post-high-temperature annealing the 8.5 nm sample after RTA to 850 °C also showed similar integrity of Al2O3 oxide thickness of 4.5 nm. A sharp transition from crystalline semiconductor interface, oxide thermal stability, and average oxide thickness of 4.5 nm. A sharp transition from crystalline InGaAs to GGO was observed, and GGO and Al2O3 remain oxide of Gd2O3 remained as high as 4 nm.

Figure 3(a) exhibits leakage current densities of 3.1 × 10⁻⁵ and 2.5 × 10⁻⁹ A/cm² at Vₜ = Vₜₖ + 1 V for the 4.5 and 8.5 nm GGOs, respectively. The low electrical leakage demonstrates the excellent thermodynamic stability, the high quality, and integrity of Al2O3/GGO dual oxide after air exposure and post-high-temperature annealing (800–850 °C).

Figure 3(b) shows the HRTEM image of the thinnest sample, indicating an atomically sharp, smooth oxide/semiconductor interface, oxide thermal stability, and average oxide thickness of 4.5 nm. A sharp transition from crystalline InGaAs to GGO was observed, and GGO and Al2O3 remain amorphous, even after air exposure and high-temperature annealing. The results indicate that GGO, as thin as ~1 nm EOT, is highly thermodynamically stable as long as it is moisture-free, similar to or even better than our previous results on thicker oxides (≥20 nm). HRTEM studies on the 8.5 nm sample after RTA to 850 °C also showed similar behavior (not shown).

When Ga2O3(Gd2O3) was thinner than 10 nm and without protection, we have previously found that its dielectric constant is much less than the value measured in the films thicker than 20 nm. For example, a κ value of 9 was obtained for 5.7 nm GGO deposited on GaAs, despite the application of an UHV annealing. Ex situ deposited ~2–3 nm thick Si3N4 as a cap on 7–8 nm thick GGO has led to a working inversion-channel InGaAs MOSFET, yet the EOT of GGO remained as high as 4 nm.

In conclusion, our results unambiguously demonstrated the attainment of high-quality bulk and interfacial properties of Al2O3/Ga2O3(Gd2O3)/In0.53Ga0.47As/GaAs after a stringent test of RTA up to 800–850 °C, one common way for fabricating inversion-channel MOSFETs. The achieved excellent electrical characteristics after the high-temperature RTA are even superior to our previous results of thicker Ga2O3(Gd2O3), and are among the best in the high-κ/III-V systems. Furthermore, Ga2O3(Gd2O3) remains amorphous withstanding annealing to 850 °C as well as maintaining atomically smooth interfaces with InGaAs. Hence, the in situ Al2O3 cap plays a vital role in extending our earlier success of unpinning surface Fermi level in the III-V’s to an aggressive scaling Ga2O3(Gd2O3) down to ~1 nm EOT, enhancing the prospect for realistic device applications. Future work includes further thinning of the in situ Al2O3 capping layer and/or in situ deposition of metal gates.

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