科目：固態電子元件(500I)

校系所組：中大電機工程學系(固態組)
交大電子研究所(甲組)
清大電子工程研究所
清大工程與系統科學系

1. Two impurities, A_1 and A_2, are uniformly doped in crystal silicon, and the energy states of the two impurities, E1 and E2, are shown in Fig.1. Assume the intrinsic density, $n_i = 1\times10^{10}$ cm^{-3}.
   (a) Which impurity is acceptor? Which impurity is donor? (5%)
   (b) Assume the two impurities are fully ionized, A_1's concentration is 5×10^{17} cm^{-3} and A_2 is 1×10^{18} cm^{-3}, what are the electron and hole concentrations in the silicon (cm^{-3})? (5%)
   (c) If without proper annealing process, the ionization rate of A_1 reduces to 50% and that of A_2 reduces to only 10%, what are the electron and hole concentrations (cm^{-3})? (5%)

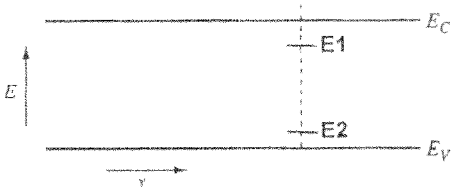

Fig. 1

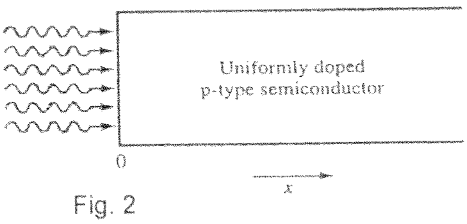

Fig. 2

2. For a p-type silicon as shown in Fig.2, and there is a continuous uniform electron current flowing from the left to the right. Answer the following questions.
   (a) If electron mobility remains constant with temperature, how does the diffusivity, D_n, change with temperature? Any why? (5%)
   (b) Explain what govern the minority lifetime (τ_n) in a semiconductor material and how does τ_n affect the diffusion process? (5%)
   (c) Let electron density $\mathbf{n(x=0)= n_o}$. Write down the expression of the electron concentration at $x > 0$, where the diffusion lengths are L_n for electrons and L_p for holes. (5%)

3. Consider one n-type and one p-type crystal silicon have same doping concentration, 10^{16}cm^{-3} and the impurities are fully ionized at room temperature. (μ_n = 1200 cm^2/V•s and μ_p = 450 cm^2/V•s)
   (a) Let the p-type silicon with length of 8cm and the cross-sectional area is 1cm^2 and the n-type silicon has same cross-sectional area and resistance as the p-type silicon, what is the length of the n-type silicon? (5%)
   (b) There is an extra collision event (μ_x) added and which is affecting the electron conduction only. If the new total mobility of electron become μ_n =600 cm^2/V•s. What is the mobility of the extra collision event (μ_x) for electron? (5%)

4. For a silicon (bandgap 1.1 eV) one-sided abrupt P$^+$-N junction under zero bias and room temperature:
   (a) (4%) Give an expression for the depletion layer width using the built-in potential V_{bi} and the N-type doping N_D.
   (b) (4%) If the Fermi level is 0.2 eV higher than the mid-gap in the neutral N-type region, find V_{bi}.
   (c) (2%) If the P$^+$-N junction is reverse-biased, the junction capacitance will become larger, smaller, or unchanged?

注意：背面有試題

科目：固態電子元件(5001)　　校系所組：中大電機工程學系(固態組)
交大電子研究所(甲組)
清大電子工程研究所
清大工程與系統科學系

5. A silicon (bandgap 1.1 eV) P-N junction at thermal equilibrium can be separated into three distinct regions: (i) the quasi-neutral region with a constant doping N_A on the p-side; (ii) the depletion region around the junction; and (iii) the quasi-neutral region with an exponential impurity distribution on the n-side: $N_D(x) = N_{DO}\exp(-x/\lambda)$. Here, N_{DO} is constant; λ is constant and is smaller than the length of the n-side; and $x = 0$ represents the depletion edge of the n-side.
   (a) (5%) Draw the energy band diagram of the junction at thermal equilibrium (quasi-Fermi levels must be included).
   (b) (5%) The built-in electric field is developed across the quasi-neutral region in n-side. Derive an analytic expression for this field.

6. For a silicon P-N junction at 300K, the typical I-V characteristic at reverse bias is shown in the Fig.3.
   (a) (5%) Please explain the reason why the leakage current increases with the increase of reverse bias.
   (b) (5%) Please sketch the I-V characteristics of the same P-N junction at 350K, 400K, and 500K schematically.

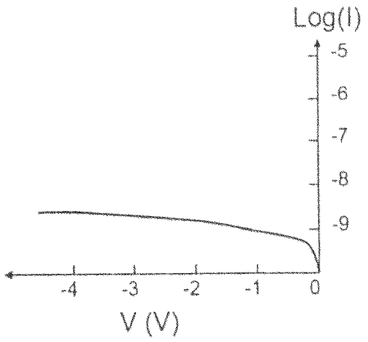

Fig. 3

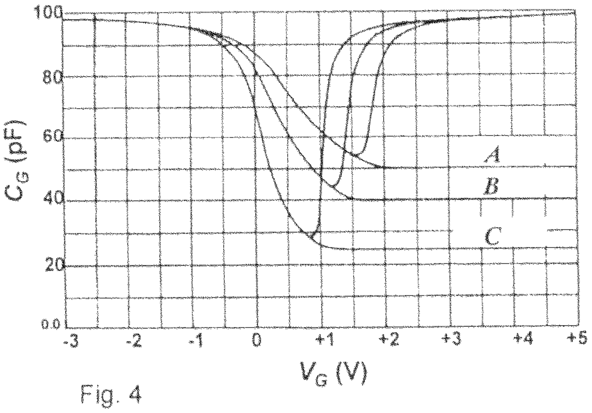

Fig. 4

7. Fig. 4 shows the measured C-V curves of n^+ - *poly-Si/SiO₂/Si* MOS capacitors. Assume that MOS capacitors ***A***, ***B***, and ***C*** have identical fabrication process and layout geometry except for different substrate doping levels, 10^{15} cm^{-3}, 10^{16} cm^{-3}, 10^{17} cm^{-3}, respectively.
   (a) What is the type (*n* or *p*) of the substrate dopant? (3%)
   (b) Which curve belongs to device ***A***? why? (6%)
   (c) What is the surface potential of device ***B*** when it is biased at threshold voltage. Plot the corresponding band diagram assuming that *poly-Si* is so heavily doped that it can be taken to be a metal. (6%)

8. Consider an n-MOSFET ($L_g = 0.1$ μm) with a uniformly doped p-substrate (N_a),
   (a) How will the threshold voltage change with increasing N_a? Provide qualitative explanation. (5%)
   (b) How will the subthreshold swing S ($\delta V_{GS} / \delta \log I_D$) change with increasing N_a? Provide qualitative explanation. (5%)
   (c) How will the drain-induced barrier lowering (DIBL) change with increasing N_a? Provide qualitative explanation. (5%)