A new share-buffered direct-injection readout structure for infrared detector

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ABSTRACT

A new current readout circuit for infrared (IR) detectors, called the Share-Buffered Direct-injection (SBDI) circuit, is proposed and analyzed. It is found that the proposed SBDI readout structure can achieve the high readout performance as the conventional Buffered Direct-Injection structure (BDI), but only with half chip area and power dissipation. A new output stage with a dynamic discharge structure is also used to overcome the conventional readout speed bottleneck. It is clearly shown through the analysis that the proposed SBDI structure and the associated design technique can be applied to the readout circuit design of the two-dimensional focal plane array and achieve the same performances as the one-dimensional BDI structure.

1. INTRODUCTION

It is well known that the Buffered Direct-Injection (BDI) readout structure for infrared (IR) detectors has a better injection efficiency due to higher transconductance, lower noise, and greater tolerance to low RoA product than the Direct-Injection (DI) structure. But the BDI has a pitch limit problem due to the additional chip-area cost paid for the differential-type buffer. Moreover, it requires more chip area and more power dissipation as compared to the DI structure. Therefore, the BDI is not suitable for the readout circuits in the 2-dimensional IR detector array.

In this paper, a new readout circuit called the share-buffered direct-injection (SBDI) readout circuit is proposed. It can achieve the requirements of high injection efficiency, low noise, small size, low power dissipation, good threshold uniformity, and cryogenic operations. The dominant power dissipation in the SBDI readout circuit is consumed by the output stage. It can be stable further decreased by using a new dynamic discharging source follower stage. The design and the performance evaluation of the SBDI readout circuit are also described in this paper.

2. SHARE-BUFFERED DIRECT-INJECTION READOUT STRUCTURE

The buffer of the new SBDI readout circuit is a differential amplifier with a shared half circuit. The circuit is shown in Fig. 1, where a dynamic discharging output stage with the auto-clamping option is also
Fig. 1. The Share-Buffered Direct-Injection (SBDI) readout structure with dynamic discharging output stage and auto-clamping option.

included. As shown in Fig. 1, the common left half circuit is composed of Q1, Q3 ∼ Q3c, and Qb, whereas the right half circuit in each cell is composed of Q2, Q4 ∼ Q4c and Qb,cell. The actual buffer in each cell is only one right half circuit of differential pair and three global lines Vbl, CS and CG. The superfluous current bias gate Qb-cell in each cell is used for the compensation of mismatching and route loading. This shared buffer structure can achieve a high injection efficiency as the BDI readout circuit. The injection efficiency η(s) and bandwidth $f_{BW}$ can be represented by

$$\eta(s) = \frac{(1 + A)g_mR_D}{1 + (1 + A)g_mR_D} \left( \frac{1}{1 + s/2\pi f_{BW}} \right)$$

$$f_{BW} = \frac{1 + (1 + A)g_mR_D}{2\pi R_D C_T}$$

where $g_m$ is the transconductance of the input MOS device Qin, $A$ is the gain of the shared buffering amplifier, $C_T$ is the total input shunting capacitance, and $R_D$ is the total input resistance of the IR detector. The gain $A$ in Eqs. (1a) and (1b) is about 100, which can be obtained through the suitable design of the shared buffering amplifier. Thus the injection efficiency $\eta$ is nearly 1 if $\omega/2\pi f_{BW} << 1$. Besides the high injection efficiency, the advantageous features in the BDI structure such as low noise and good threshold uniformity can be achieved in this SBDI current readout technique.

The series devices Q3b, Q3c, Q4b, and Q4c at the sources of the current mirror devices Q3 and Q4 are used to obtain the proper output dc bias. The reset coupling effect is isolated from the detector bias.
node by adding cascode device $Q_{cas}$ to the input device $Q_{in}$. An anti-blooming control implemented by the device $Q_{atb}$ is also included, which is turn on if the voltage on the integrating capacitor $C_{int}$ is greater than $V_{cas} + V_T$. The integrating voltage can be increased by using unbalanced amplifier input devices so that the resultant offset can turn on the input device $Q_{in}$. Hence, the dynamic range can be improved by increasing the signal level under the same noise quantity. For a 10V supply $V_{dd}$, the common voltage $V_{com}$ is chosen to be 8V and the bias $V_{cas}$ is 6V. In this case, the maximum integrated signal level on $C_{int}$ can be 7.5V. Through the transmission gate controlled by $Select$ and $Select^*$, the integrated signal is sampled to the output stage after an integration time interval.

The average power dissipation of each buffer in this SBDI input stage is calculated as 
\[ i_d (V_{dd} - V_{ss}) + \frac{i_d}{n} (V_{dd} - V_{ss}) \] where $i_d$ is the bias current in each half differential pair circuit and $n$ is the total cell number sharing the other common half differential pair circuit. As compared to the BDI structure whose power dissipation is $2i_d (V_{dd} - V_{ss})$ in each buffer, the SBDI has only nearly half of the power dissipation of the BDI. Moreover, each buffer in the SBDI is implemented by only half device count of the BDI and thus it needs only half chip area. The low heat loading per unit cell and the small size in the SBDI make it much more suitable than the BDI for the application to the readout circuit of high performance and integrity 2-D IR focal plane array (FPA).

### 3. DYNAMIC DISCHARGING OUTPUT STAGE

The new output stage is implemented by a NMOS source follower consisting of $Q_5$ and $Q_6$ with a dynamic discharging device $Q_{dy}$ as shown in Fig. 1. The operation of the output stage is described below. First, the current signal is integrated to a high voltage level on the capacitor in each cell and the output stage node is preset to low. When the transmission gate is ON, $Q_5$ has a high gate-to-source voltage and generates a large charge current to push the output high. Then, the clock $Reset$ is high and the integration capacitor is reset to $V_{ss}$. At this time, the device $Q_5$ turns OFF and the output node is pulled to low by a constant current of $Q_6$. Through the analysis, clearly the discharging phase is the speed bottleneck of the output stage. The dynamic discharging device $Q_{dy}$ controlled by the clock $Dyrs$ is used to overcome the speed limit and the output is pulled to low quickly by dynamically turning on $Q_{dy}$ in the reset phase. This dynamic discharging output stage consumes only dynamic power and can drastically decrease the power dissipation of the output stage, which always dominates the total power consumption of the readout chip. According to the SPICE simulation results, a 1MHz readout speed with low power dissipation can be achieved with 25pF output loading.

The additional clock $Dyrs$ can be shared by the correlated-double sampling (CDS) stage that eliminates the $1/f$ noise by a capacitor $C_{cds}$ and a sampling gate $Q_{cds}$ as shown in Fig. 2. In this structure, the dynamic discharging device $Q_{dy}$ is moved to the last stage after the CDS circuit to pull down the off-chip loading and improve the speed performance. An auto-clamping structure is formed by connecting the source node of $Q_6$ to a clamping voltage $V_{cclp}$. This clamping voltage is sampled to the capacitor $C_{cds}$ in the first pre-reset phase of CDS. When signal is sampled to the output stage at the second sample phase of the CDS, it can be subtracted by the clamping voltage on $C_{cds}$ and achieves an on-chip auto-clamping function. This auto-clamping function can subtract a tunable DC background level in order to do an off-chip post amplification. It is also optional to connect $V_{cclp}$ to $V_{ss}$. 
4. SIMULATION AND EXPERIMENTAL RESULTS

The SPICE simulation results of the current readout in the SBDI with the input signals 25nA, 50nA, 75nA, 100nA, 125nA and the saturation level are shown in Figs. 3 and 4. The maximum integrated voltage level controlled by the anti-blooming gate can reach 7.5V as shown in Fig. 3. The output waveform of the SBDI readout with a dynamic discharge output stage and clamping option is shown in Figs. 4(a) and 4(b). The charging and discharging speed can be improved by slightly enlarging the (W/L) ratio of Q5 and Qdy in Fig. 1. The clamping voltage is chosen according to the background current level. If the background current level is larger than 50nA, we can choose the clamping voltage as 2V and the background DC level is clamped to be 2V as shown in Fig. 4(b). This background DC level can be subtracted in the CDS stage. The auto-clamping function can be omitted if the signal level under 50nA is to be detected. Because of the gate-to-source voltage drop of the NMOS source-follower, the signal level under 20nA is not detectable. This readout technique is suitable for a high background low signal environment.

8x1 and 64x1 SBDI readout chips have been designed, and fabricated in 3μm CMOS process. The layout diagram of 8x1 and 64x1 SBDI chips are shown in Figs. 5 and 6, respectively. A linearity performance of the SBDI readout circuit with and without the CDS stage is shown in Fig. 7. The dc level difference between Vout and Vout(CDS) is due to the gate-to-source drop of the NMOS source-follower as the unity-gain buffer. The test performance is summarized in Table. I, where the power dissipation is calculated for the 64x1 SBDI readout chip.
5. CONCLUSIONS

A high performance SBDI IR current readout structure has been demonstrated and analyzed. Using the SBDI structure, the power dissipation and chip area problems of the BDI can be solved. Moreover, a new output stage with dynamic discharging structure is designed to improve readout speed and avoid static power dissipation. The inherent advantages of low power and small chip area in the SBDI current readout structure make it suitable for the application to the high performance 2-dimensional IR FPA readout.

6. REFERENCES

Fig. 3. The integrated voltage on Cint with input 25nA, 50nA, 75nA, 100nA, 125nA and saturation.

(a)

(b)

Fig. 4. The output voltage waveform with the input current of (a) 25nA, 50nA, 75nA, 100nA, 125nA, and the saturation level with Vclp=0V; (b) 50nA, 75nA, 100nA, 125nA, and the saturation level with Vclp=2V.
Fig. 5. The 8x1 SBDI readout chip layout.

Fig. 6. The 64x1 SBDI readout chip layout.
Table I.
Test results and operation condition for the share-buffered direct-injection current readout structure

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Results</th>
</tr>
</thead>
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<tr>
<td>Power supply</td>
<td>0-10V</td>
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<tr>
<td>Max. Photo-current</td>
<td>130 nA</td>
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<tr>
<td>Max. Readout speed</td>
<td>1 MHz</td>
</tr>
<tr>
<td>Integration capacitance</td>
<td>&gt; 2 pF</td>
</tr>
<tr>
<td>Storage capacity</td>
<td>&gt; 1.0 x 10^8 e^-</td>
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<tr>
<td>Transimpedance</td>
<td>&gt; 40 MΩ</td>
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<tr>
<td>Power dissipation</td>
<td>&lt; 10 mW</td>
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<tr>
<td>Linearity</td>
<td>&gt; 98%</td>
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<tr>
<td>Anti blooming control</td>
<td>yes</td>
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<tr>
<td>Operation temperature</td>
<td>77° k</td>
</tr>
</tbody>
</table>

Fig. 7. The linearity performance of the SBDI readout structure with input from 50nA to 125nA and a step 5nA (with and without the on-chip CDS)