The positive bias temperature instability of n-channel metal-oxide-semiconductor field-effect transistors with ZrO2 gate dielectric

De-Cheng Hsu, Ingram Yin-ku Chang, Ming-Tsong Wang, Pi-Chun Juan, Y. L. Wang et al.

Citation: Appl. Phys. Lett. 92, 202901 (2008); doi: 10.1063/1.2928235
View online: http://dx.doi.org/10.1063/1.2928235
View Table of Contents: http://apl.aip.org/resource/1/APPLAB/v92/i20
Published by the American Institute of Physics.

Related Articles
Charge transport in dual-gate organic field-effect transistors
Top-gate thin-film transistors based on GaN channel layer
Charge transport in dual-gate organic field-effect transistors
Solid polyelectrolyte-gated surface conductive diamond field effect transistors
Percolation model for the threshold voltage of field-effect transistors with nanocrystalline channels

Additional information on Appl. Phys. Lett.
Journal Homepage: http://apl.aip.org/
Journal Information: http://apl.aip.org/about/about_the_journal
Top downloads: http://apl.aip.org/features/most_downloaded
Information for Authors: http://apl.aip.org/authors
The positive bias temperature instability of n-channel metal-oxide-semiconductor field-effect transistors with ZrO2 gate dielectric

De-Cheng Hsu,1 Ingram Yin-ku Chang,1 Ming-Tsong Wang,a,b Pi-Chun Juan,3 Y. L. Wang,2 and Joseph Ya-min Lee
1Department of Electrical Engineering and Institute of Electronics Engineering, National Tsing-Hua University, Hsinchu, Taiwan 300, Republic of China
2Taiwan Semiconductor Manufacturing Company. No. 25, Li-Hsin Rd., Science-Based Industrial Park, Hsin-Chua, Taiwan 300, Republic of China
3Department of Materials Engineering, Mingchi University of Technology, 84 Guangjuan Rd., Taishan, Taipei, Taiwan 243, Republic of China

(Received 30 July 2007; accepted 16 April 2008; published online 19 May 2008)

The positive bias temperature instability of n-channel metal-oxide-semiconductor field-effect transistors with ZrO2 gate dielectric was studied. It was observed that the degradation in threshold voltage (ΔVT) has an exponential dependence on the stress time in the temperature range from 25 to 75 °C. The measurement of subthreshold slope (ΔS) during stress indicates that the degradation in VT is due to the interface trap charges Qit. The extracted activation energy of 0.3–0.5 eV is related to a degradation dominated by the release of atomic hydrogen in the Si–ZrO2 interface. © 2008 American Institute of Physics. [DOI: 10.1063/1.2928335]

Recently, high-k dielectrics have attracted great attention. Zirconium oxide (ZrO2) is a potential candidate due to its high dielectric constant (20–25),1–3 large energy band gap (5.4 eV), high breakdown electric field (7–15 MV/cm), and low leakage current level.1–3 Positive bias temperature instability (PBTI) in high-k films is an important subject for these applications. Zhang and Eccleston4,5 investigated the PBTI of submicrometer metal-oxide-semiconductor field-effect transistors (MOSFETs) with SiO2 gate dielectric. An activation energy of 1.23 eV was extracted. Shen et al.6 observed the charge trapping effect of HfO2 gate dielectric and related the effect to oxygen vacancies after bias temperature instability test. Onishi et al.8 reported that the threshold voltage degradation in PBTI in nMOSFETs was primarily caused by charge trapping in HfO2 rather than interfacial degradation. Compared with HfO2, there were few studies on PBTI and stress-induced leakage current mechanisms of ZrO2-gated transistors. In our previous study, the time dependent dielectric breakdown of ZrO2 capacitors was studied.7 In this work, n-channel MOSFETs with ZrO2 gate dielectric were fabricated and the PBTI characteristics were studied.

P-type, (100) orientation, silicon wafers (1–10 Ω cm) were used as the starting material. The ZrO2 thin films were deposited by radio frequency magnetron sputtering in argon at room temperature. A rapid annealing was performed at 500 °C for 60 s in nitrogen with a flow rate of 3 cm3/min (SCCM) (SCCM denotes cubic centimeter per minute at STP).

The top electrode is aluminum. The channel width is 100 μm and the channel length varies from 3 to 20 μm. The thickness of ZrO2 films varies from 7.5 to 20 nm and the dielectric constant is 18.0 as measured from separate metal-insulator-semiconductor capacitors. All the I–V and I–t measurements of Al/ZrO2/p-Si MOS capacitors and transistors were carried out using Keithly 236.

PBTI tests were performed on nMOSFETs with a positive bias stress ranging from 1 to 5 V and measured in the temperature range from 25 to 75 °C. The top electrode was positively biased. The source, drain, and substrate contacts were all grounded. The threshold voltage VT can be written as

\[ V_T = \phi_{ms} - \frac{Q_I + Q_{ox} + Q_m + Q_{it}}{C_{ox}} + 2\psi_B + \frac{\sqrt{4e_0\xi NA_{m}^{+}}}{C_{ox}}, \]

where \(q\phi_{ms}\) is the work function difference between aluminum and silicon, \(Q_I\) is fixed oxide charge, \(Q_m\) is mobile ionic charge, \(Q_{ox}\) is oxide trapped charge, \(Q_{it}\) is interface trapped charge, and \(\psi_B\) is the energy difference between the Fermi level \((E_f)\), and the intrinsic Fermi level \((E_i)\) in silicon. Because \(\phi_{ms}, Q_m, Q_{it}, N_A, C_{ox}\), and \(\psi_B\) are essentially stress independent, the degradation in the threshold voltage \(\Delta V_T\) is mainly due to the trapped charges, namely \(Q_{ox}\) and \(Q_{it}\).

Figures 1(a) and 1(b) show the degradation in threshold voltage \(\Delta V_T\) versus stress time of nMOSFETs at 25 and 75 °C, respectively. \(V_T\) decreases with stress time and, therefore, \(\Delta V_T\) is negative. This can be explained by an increase in positive trapped charges with stress time. The degradation in the threshold voltage follows an empirical equation of \(\Delta V_T = at^n\), where \(a\) is a constant, \(t\) is the stress time, and \(m\) is the exponent which is equal to \(m_1\) or \(m_2\) in the linear \((t < 300 \text{ s})\) or saturation \((t > 300 \text{ s})\) regions, respectively.11

Since \(m_2\) is much smaller than \(m_1\) at both 25 and 75 °C, few traps are generated for \(t > 300 \text{ s}\). The values of \(m_1\) at 25 °C are in the range of 0.15–0.46 which are larger than those at 75 °C between 0.13 and 0.18. Furthermore, the \(\Delta V_T\) value is larger at 25 °C than that at 75 °C. This can be explained by a higher probability of electron-hole recombination at the higher temperature of 75 °C and hence less oxide trapped charges.4

---

aElectronic mail: mtwang@tsmc.com.
The threshold voltage shift ($\Delta V_T$) due to PBTI, given by the reaction-diffusion ($R\cdot D$) model, can be written as:

$$\Delta V_T = \Delta V_{\text{max}} \{1 - \exp\left(-\left(\frac{t}{\tau_0}\right)^\beta\right)\},$$

where $t$ is the stress time, $\Delta V_{\text{max}}$ is the maximum $\Delta V_T$ and related to the total trap density, $\epsilon$ is the permittivity of the dielectric, $A$ is the gate area, $(d)$ is the centroid of trapped charges, and $\beta$ is the distribution width. $\tau_0$, $\Delta V_{\text{max}}$, and $\beta$ are fitting parameters. The curve-fitted values of $\beta$ from the $V_T$ shift versus stress time plot in Figs. 1(a) and 1(b) are from 0.41 to 0.55 at 25 °C and from 0.22 to 0.30 at 75 °C. Larger $\beta$ implies smaller capture cross section and more trapped charges. The distribution width $\beta$ decreases with increasing temperature. This suggests a higher probability of electron-hole recombination at high temperature of 75 °C.

In order to clarify whether $Q_{\text{ot}}$ or $Q_{\text{dt}}$ gives rise to the negative threshold voltage shift, both the gate leakage current $I_G$ and the subthreshold slopes $S$ under constant voltage stress from 1 V ($E=0.58$ MV/cm) to 5 V ($E=2.89$ MV/cm) and in the temperature range from 25 to 75 °C are analyzed. The subthreshold slope $S$ is given by:

$$S = 2.3 \frac{kT}{q} \left[1 + \frac{C_d + C_{\text{de}}}{C_i}\right],$$

where $C_i$ is the gate capacitance, $C_d$ is the depletion capacitance, and $C_{\text{de}}=qD_{\text{in}}$ is the fast interface state capacitance. Because $C_i$ and $C_d$ are essentially bias temperature independent, $\Delta S$ depends only on $Q_{\text{dt}}$. Figures 2(a) and 2(b) show the variations of the subthreshold slope ($\Delta S$) with stress time at 25 and 75 °C, respectively. $m_3$ and $m_4$ are the slopes of the $\Delta S/S$ (%) versus stress time plot in the linear ($t<300$ s) and saturation ($t>300$ s) regions, respectively. The degradation in the threshold voltage ($\Delta V_T$) and the subthreshold slope ratio ($\Delta S/S$) with stress time shows a similar trend. Since $\Delta S$ depends only on $Q_{\text{dt}}$, this suggests that the degradation in $V_T$ is due to the interface traps $Q_{\text{dt}}$. Figure 3 shows the gate leakage of ZrO2-gated nMOSFETs under a constant stress voltage of 2 V. If there are more positive oxide trapped charges $Q_{\text{ot}}$ in ZrO2, the gate leakage current $I_G$ will increase with increasing $Q_{\text{ot}}$ due to the increase in the electric field in the dielectric. However, the gate-leakage current $I_G$ is found to vary much less with increasing stress time. This suggests that the positive trapped charges generated during the stress process are not oxide trapped charges $Q_{\text{ot}}$. 

![Figure 1](image1.png)  
**FIG. 1.** The $V_T$ shift of ZrO2-gated nMOSFETs as a function of stress time (a) at a stress temperature of 25 °C. (b) at a stress temperature of 75 °C. The La2O3 thickness is 17.3 nm. The channel width and length are 100 and 8 μm, respectively.

![Figure 2](image2.png)  
**FIG. 2.** The percent degradation of subthreshold swing ($\Delta S/S$) as a function of stress time for ZrO2-gated nMOSFETs (a) at a stress temperature of 25 °C. (b) at a stress temperature of 75 °C.

![Figure 3](image3.png)  
**FIG. 3.** The gate leakage current of ZrO2-gated nMOSFETs after a constant stress voltage of 2 V applied for various time periods from 0 to 1000 s at 25 and 75 °C. The ZrO2 thickness is 17.3 nm. The channel width and length are 100 and 8 μm, respectively. The area of MOS capacitors is 3.14 × 10⁻⁴ cm². The inset graph shows the plot of $\Delta V_T$ as a function of reciprocal temperature (1/kT).
In the R-D model, the temperature-dependent threshold voltage shift ($\Delta V_T$) can be expressed as \[^{11,13-15}\]

$$\Delta V_T \propto \exp[-(\alpha E_{ox} - E_a)/kT],$$

(5)

where $E_{ox}$ is the electric field, $E_a$ is the activation energy, and $\alpha$ is the polarization parameter. The activation energy ($E_a = E_{diss}/2 - E_m/4$) is the sum of the dissociation energy of the reaction ($E_{diss}$) and the migration energy of hydrogen diffusion ($E_m$).\[^{13-15}\] Both the reaction and diffusion terms contribute to the measured activation energy. For a degradation dominated by the release of atomic hydrogen at the Si–SiO$_2$ interface, the activation energy is 0.2 eV.\[^{13-15}\] In order to clarify the origin of the positive trapped charges, the logarithm of the threshold voltage shift [$\Delta V_T$] is plotted as a function of inverse temperature in the inset of Fig. 3. The extracted activation energy is 0.3–0.5 eV for gate voltages from 2 to 3 V. This activation energy is on the same order of magnitude as the energy of 0.2 eV. This suggests that the activation energy of 0.3–0.5 eV might be related to a degradation dominated by the release of atomic hydrogen at the Si–ZrO$_2$ interface. Similar phenomena were observed for SiO$_2$ and HfO$_2$ films.\[^{4,13,14}\] This also suggests that the degradation in $V_T$ is due to the interface traps $Q_{it}$.

In summary, the PBTI effect of Al/ZrO$_2$/p-Si nMOSFETs was studied. The degradation in threshold voltage ($\Delta V_T$) has an exponential dependence on the stress time up to 300 s in the temperature range from 25 to 75 °C. The measurement of subthreshold slope ($\Delta S$) with stress shows that the degradation in $V_T$ is due to the interface trap charges $Q_{it}$. The extracted activation energy of 0.3–0.5 eV is most likely related to the release of atomic hydrogen at the Si–ZrO$_2$ interface.

The authors would like to thank the National Science Council, Taiwan, Republic of China for supporting this work under Contract No. NSC96-2221-E-007-160-MY2.


