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Citation: Appl. Phys. Lett. 91, 203517 (2007); doi: 10.1063/1.2805218
View online: http://dx.doi.org/10.1063/1.2805218
View Table of Contents: http://apl.aip.org/resource/1/APPLAB/v91/i20
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The electrical and interfacial properties of metal-high-\(k\) oxide-semiconductor field effect transistors with CeO\(_2\)/HfO\(_2\) laminated gate dielectrics

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(Received 6 September 2007; accepted 14 October 2007; published online 16 November 2007)

Metal-oxide-semiconductor field-effect transistors with CeO\(_2\)/HfO\(_2\) laminated gate dielectrics were fabricated. The transistors have a subthreshold slope of 74.9 mV/decade. The interfacial properties were measured using gated diodes. The surface state density \(D_\text{it}\) was 4.9 \(\times\) 10\(^{11}\) cm\(^{-2}\) eV\(^{-1}\). The surface-recombination velocity \(S\) measured was 4 \(\times\) 10\(^{12}\) cm/s and the effective capture cross section \(\sigma_c\) extracted was about 7.69 \(\times\) 10\(^{-15}\) cm\(^2\). The effective mobility of CeO\(_2\)/HfO\(_2\) laminated gate transistors was determined to be 212 cm\(^2\)/V s.

Recently, high-\(k\) dielectrics have attracted great attention. Hafnium oxide (HfO\(_2\)) and cerium oxide (CeO\(_2\)) are potential candidates for these applications. HfO\(_2\) has high dielectric constant (21–30), large energy band gap (5.8 eV), and high thermal stability, has received major attention as dielectric.\(^1\)–\(^5\) Another promising candidate is CeO\(_2\) which has high dielectric constant (20–26), large energy band gap (5.5 eV), and very low lattice mismatch (0.35%) with silicon.\(^6\)–\(^9\) The very low lattice mismatch of CeO\(_2\)/Si interface is of great help in improving the interface properties of the high-\(k\) devices for future very large scale integration applications. In the literature, Nishikawa et al.\(^10\) showed that a leakage current density at electrical field of 5 MV/cm for the CeO\(_2\) metal-insulator-semiconductor capacitors was about 1 A/cm\(^2\). Karakaya et al.\(^11\) reported that the low fixed-charge density \(Q_F\) was 4 \(\times\) 10\(^{12}\) cm\(^{-2}\) and the low leakage current density \(J_F\) was 1.9 \(\times\) 10\(^{-7}\) A/cm\(^2\) for the laminated CeO\(_2\)/HfO\(_2\) gate dielectrics. However, some of the laminated high-\(k\)/Si interface properties such as the effective capture cross section and the surface-recombination velocity have not been fully addressed.

In this work, \(n\)-channel metal-oxide-semiconductor field-effect transistors (\(n\)MOSFETs) with CeO\(_2\)/HfO\(_2\) laminated gate dielectrics were fabricated. Electrical measurements were performed using Al/HfO\(_2\)/CeO\(_2\)/\(p\)-Si structures. The subthreshold-swing measurement\(^12\) and gated diode measurement\(^3,14\) were utilized to analyze the high-\(k\)/Si interfacial characteristics.

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![Image](https://example.com/image.jpg)

**FIG. 1.** The \(I_{\text{DS}}-V_{\text{GS}}\) characteristics of \(n\)MOSFETs with CeO\(_2\)/HfO\(_2\) laminated gate dielectrics at various gate voltages \(V_{\text{GS}}\). The inset shows the high-frequency (1 MHz) C-V curve of CeO\(_2\)/HfO\(_2\) laminated MOS capacitor annealed at 400 °C in nitrogen for 60 s.
CeO$_2$/HfO$_2$ laminated gate dielectrics is about 212 cm$^2$/V s.

About the laminated high-$k$/Si interface properties, the gated diodes were used to measure the surface-recombination velocity ($s_0$), the minority carrier lifetime in the field-induced depletion region ($\tau_{0,\text{FL}}$), and the effective capture cross section of surface state ($\sigma_{t}$). The inset of Fig. 3 shows the setup of the gated diode measurement and the three distinct regions of $I_{RS}$ measurements. The drain is reverse biased with respect to the substrate ($V_D=V_{DB}$). When the gate voltage ($V_G$) is less than the flatband voltage ($V_{FB}$), the high-$k$/Si interface is in the accumulation mode and the reverse diode current ($I_R$) is due to the generation-recombination (G-R) centers in the depletion region of the metallurgical junction ($I_{gen,MJ}$). When $V_{FB}V_GV_T$ (threshold voltage), the field-induced junction is depleted and the abrupt increase of the reverse current originates from the generation of the electron-hole pairs at the generation-recombination centers of the field-induced junction depletion region ($I_{gen,FL}$) and the surface region ($I_{gen,s}$). At $V_TG$, the field-induced region is in the inversion and the reverse current is reduced by filling the interface states with the minority carriers. Figure 3 shows the $I_{RS}$ gated diode characteristics of the MOSFETs with CeO$_2$/HfO$_2$ laminated gate dielectrics. The equations of the gated diode are written as

$$I_{gen,MJ} = qU_{MJB}A_M W,$$

$$I_{gen,s} = \frac{qN AS_0}{2},$$

where $U_{MJB}$ and $U_{FL}$ are G-R rates of the carriers per unit volume in the depletion region of the metallurgical junction and in that of the field-induced junction, respectively, $A_M$ and $A_g$ are the areas of the metallurgical junction and the gate, respectively; $n_i=1.45 \times 10^{10}$ cm$^{-3}$ is the intrinsic carrier concentration of Si, $W$ is the width of the depletion region of the metallurgical junction, $W_{d,max}$ is the maximum width of the surface depletion region, $\tau_{0,FL}$ is the minority carrier lifetime in the depletion region of the field-induced junction, $s_0$ is the surface-recombination velocity, $\sigma_{t}$ is the effective capture cross section, $v_{th}=10^7$ cm/s is the thermal velocity, $N_{fit}$ is the density of the single-level surface G-R centers per unit 

### Table I. A comparison of the experimental results of gated diodes with SiO$_2$, high- $k$ gate dielectrics, and CeO$_2$/HfO$_2$ laminated (this work) gate dielectrics. The $V_{FG}$ for CeO$_2$/HfO$_2$ laminated gated diodes is 3 V.

<table>
<thead>
<tr>
<th>Gate dielectrics</th>
<th>$I_{gen,MJ}$ ($A/cm^2$)</th>
<th>$I_{gen,s}$ ($A/cm^2$)</th>
<th>$I_{gen,FL}$ ($A/cm^2$)</th>
<th>$s_0$ ($cm/s$)</th>
<th>$\sigma_{t}$ ($cm^2/s$)</th>
<th>$N_{fit}$ ($cm^{-2}$)</th>
<th>$D_{th}$ ($cm^2/Vs$)</th>
<th>$\tau_{0,FL}$ ($s$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SiO$_2$¹</td>
<td>$10^{-4}$</td>
<td>$10^{-8}$</td>
<td>$1.1 \times 10^{-4}$</td>
<td>5</td>
<td>$1 \times 10^{-16}$</td>
<td>$5 \times 10^{9}$</td>
<td>$5 \times 10^{10}$</td>
<td>$10^{-5}$</td>
</tr>
<tr>
<td>Ta$_2$O$_5$⁰</td>
<td>$6.03 \times 10^{-2}$</td>
<td>$9.3 \times 10^{-3}$</td>
<td>$4 \times 10^{-8}$</td>
<td>780</td>
<td>$\cdots$</td>
<td>$9.5 \times 10^{-2}$</td>
<td>$3 \times 10^{-6}$</td>
<td>$\cdots$</td>
</tr>
<tr>
<td>HfO$_2$</td>
<td>$3.17 \times 10^{-6}$</td>
<td>$\cdots$</td>
<td>$\cdots$</td>
<td>$2728$</td>
<td>$1.6 \times 10^{-15}$</td>
<td>$1.7 \times 10^{11}$</td>
<td>$\cdots$</td>
<td>$1.13 \times 10^{-8}$</td>
</tr>
<tr>
<td>ZrO$_2$</td>
<td>$1.3 \times 10^{-6}$</td>
<td>$4.1 \times 10^{-6}$</td>
<td>$5.7 \times 10^{-6}$</td>
<td>$3.5 \times 10^{3}$</td>
<td>$5.8 \times 10^{-16}$</td>
<td>$6.0 \times 10^{11}$</td>
<td>$7.4 \times 10^{12}$</td>
<td>$2.7 \times 10^{-6}$</td>
</tr>
<tr>
<td>CeO$_2$/HfO$_2$</td>
<td>$1.4 \times 10^{-5}$</td>
<td>$7.1 \times 10^{-6}$</td>
<td>$5 \times 10^{-6}$</td>
<td>$6.11 \times 10^{3}$</td>
<td>$7.69 \times 10^{-15}$</td>
<td>$7.95 \times 10^{10}$</td>
<td>$9.78 \times 10^{11}$</td>
<td>$1.8 \times 10^{-8}$</td>
</tr>
</tbody>
</table>

¹References 12 and 18.
²Reference 19.
³Reference 20.
⁴Reference 21.
area, $D_{it}$ is the density of uniformly distributed surface $G$-$R$ centers per unit area and energy, $V_{bi}$ is the built-in potential of the $p$-$n$ junction, and $\phi_p$ is the quasi-Fermi potential of the majority carriers in the substrate.

In this work, the effective capture cross section ($\sigma_i$) and the density of interface state per area ($N_{it}$) are determined to be about $7.69 \times 10^{-15}$ cm$^2$ and $7.95 \times 10^{10}$ cm$^{-2}$, respectively. The minority carrier lifetime in the field-induced junction depletion region ($\tau_{F,ij}$) determined by the gated diode measurement is about $1.8 \times 10^{-8}$ s. The $s_0$ is about $6.11 \times 10^3$ cm/s at $V_R = 3$ V. Table I summarizes a comparison of the experimental results of gated diodes with SiO$_2$,12,13,18 CeO$_2$/HfO$_2$ laminated gate dielectrics are the lowest in comparison with other high-$k$ gated diodes. The reason of this is attributed to the very low lattice mismatch of the CeO$_2$/Si interface. The effective capture cross section of the laminated high-$k$/Si interface is about two orders of magnitude larger than that of the SiO$_2$/Si interface.

The authors would like to thank the National Science Council, Taiwan, Republic of China for supporting this work under Contract No. NSC-95-2221-E-007-243.