$Ga_2O_3(Gd_2O_3)/Si_3N_4$ dual-layer gate dielectric for InGaAs enhancement mode metal-oxide-semiconductor field-effect transistor with channel inversion

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A dual-layer gate dielectric approach for application in III-V metal-oxide-semiconductor field-effect transistor (MOSFET) was studied by using ultrahigh vacuum deposited 7–8 nm thick $Ga_2O_3(Gd_2O_3)$ as the initial dielectric to unpin the surface Fermi level of $In_{0.18}Ga_{0.82}As$ and then molecular-atomic deposition of ~2–3 nm thick Si_3N_4 as a second dielectric protecting $Ga_2O_3(Gd_2O_3)$. The total equivalent oxide thickness achieved in this study is 5 nm. We have demonstrated an enhancement mode $In_{0.18}Ga_{0.82}As/GaAs$ MOSFET with surface inverted *n* channel with drain current (I_d) of 0.1 mA for a gate length of 10 μm and a gate width of 880 μm at $V_{ds}=1$ V and $V_g=4.5$ V. © *2007 American Institute of Physics*. [DOI: 10.1063/1.2817742]

Driven by the need to apply III-V compound semiconductors with high carrier mobility as channel materials to extend Moore's law on complementary metal oxide semiconductor (CMOS) scaling beyond 22 nm node silicon,[1,2] integration of high-κ dielectrics on the III-V's has become a very important topic of research recently. To unpin the surface Fermi level by a high-κ dielectric that can be scaled to nanometer thickness has been the focus of the recent research activities.[3,4] Surface Fermi-level pinning problem had been a subject of nearly 40 years of extensive research in the past.[5] Ultrahigh vacuum (UHV) *in situ* growth of $Ga_2O_3(Gd_2O_3)$ as high-κ dielectric on GaAs was proven to unpin the surface Fermi level effectively with a low interfacial density of states comparable with that of Si/SiO_2 interface[6] and also gave low electrical leakage currents.[7] Both *n*- and *p*-channel enhancement mode GaAs and $In_{0.53}Ga_{0.47}As/InP$ metal-oxide-semiconductor field-effect transistors (MOSFETs) with inversion have been demonstrated using $Ga_2O_3(Gd_2O_3)$ as a gate dielectric.[8–10] Also, $Ga_2O_3(Gd_2O_3)$ is a high-κ material with a dielectric constant of ~15, making it very promising for embodiment in III-V channel material based CMOS circuits with scaling of equivalent oxide thickness (EOT).

However, upon air exposure, $Ga_2O_3(Gd_2O_3)$ has been found to be degraded due to absorption of moisture (H_2O).[11] With a proper heat treatment of removing the moisture in UHV or under atmosphere, $Ga_2O_3(Gd_2O_3)/GaAs$ heterostructures have been demonstrated to be thermodynamically stable and have exhibited low leakage current densities and low interfacial densities of states with annealing up to ~780 °C.[12,13] However, for minimizing degradation of the oxide/III-V interfaces during device processing, very thick gate dielectric films of ~40 nm (which is ~10 nm in EOT) have so far been used in the MOSFETs. Thick EOT limits the gate drivability. Moreover, thick dielectric films tend to have more bulk electrical active trap defects, causing large hysteresis in device operation. Thus, a way to make use of thinner $Ga_2O_3(Gd_2O_3)$ without suffering from moisture has to be designed.

In this letter, we report an approach of using thin $Ga_2O_3(Gd_2O_3)$ as the initial gate dielectric layer to unpin the Fermi level of the III-V surface and then of using Si_3N_4 as a second dielectric deposited on top of $Ga_2O_3(Gd_2O_3)$ to prevent and/or minimize moisture absorption to achieve a stable dual-layer gate dielectric. Molecular and atomic deposited (MAD) Si_3N_4 was employed because it is bulk-trap-free upon annealing at sufficiently high temperature and can be pinhole-free down to 1 nm thickness,[14] very important as a barrier for moisture. We have, thus, made a $Si_3N_4/Ga_2O_3(Gd_2O_3)$ dual-layer gate dielectric with a total EOT of 5 nm. Enhancement mode MOSFETs with channel inversion were fabricated and demonstrated to exhibit the ability of unpinning the InGaAs surface Fermi level. This is a proof of principle in a dual-layer gate dielectric approach.

Be ($5\times10^{16}/cm^3$) doped *p*-type strained 80 Å thick $In_{0.18}Ga_{0.82}As$ was grown on 5000 Å Be ($5\times10^{16}/cm^3$) doped *p*-GaAs buffer in a *p*-doped GaAs substrate. E-beam deposition of $Ga_2O_3(Gd_2O_3)$ was carried out *in situ* on top of the freshly grown $In_{0.18}Ga_{0.82}As$. The experimental procedure on growth of the oxide/semiconductor heterostructures was described earlier.[15] The wafer was then transferred to a MAD system, which is a second generation of jet vapor deposition for *ex situ* Si_3N_4 deposition.[14] Prior to Si_3N_4 deposition, wafer was heated inside the MAD system at 200 °C for 30 min to drive away unintentionally absorbed moisture inside $Ga_2O_3(Gd_2O_3)$ film during the sample

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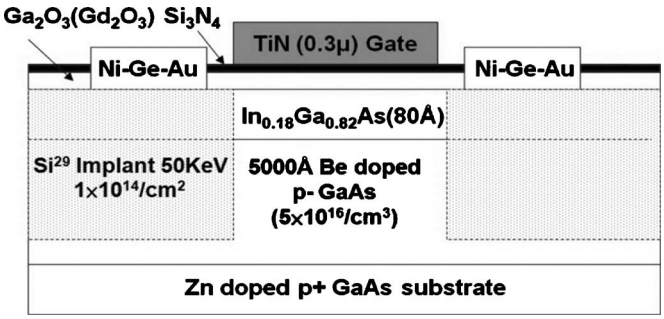

FIG. 1. A cross-sectional illustration of the enhancement mode MOSFET structure with self-aligned implant for source and drain. The Ni–Ge–Au contacts are also self-aligned to the openings from etched $Si_3N_4/Ga_2O_3(Gd_2O_3)$.

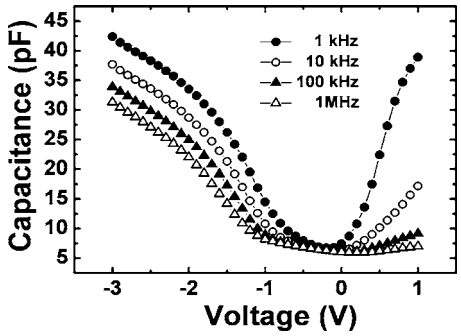

FIG. 3. *C-V* curves measured from 1 kHz to 1 MHz frequency. The lower frequency *C-V* curves show inversion characteristics of the $TiN/Si_3N_4/Ga_2O_3(Gd_2O_3)/p\text{-}In_{0.18}Ga_{0.82}As$.

transferring.[12,13] 2–3 nm thick Si_3N_4 was then deposited on top of $Ga_2O_3(Gd_2O_3)$ to form the dual-layer gate dielectric stack. The wafer stack underwent 600 °C for 15 min in N_2 and then 375 °C for 1 min in forming gas (N_2 with 4% H_2) as postdeposition annealing to improve the dielectric quality of both Si_3N_4 and $Ga_2O_3(Gd_2O_3)$.

Gate-first process was used to fabricate enhancement mode MOSFET with inverted *n* channel. Ring shaped TiN gates (0.3 μm in thickness) with a gate length L of 10–50 μm were formed by sputtered TiN followed by a lift-off patterning process. The wafer with TiN (as the gate metal) on top of $Ga_2O_3(Gd_2O_3)/Si_3N_4$ dual-layer dielectric was then implanted with 50 keV Si^{29} to a dose of $10^{14}/cm^2$. Dopant activation was performed at 800 °C 10 s in a N_2 ambient. A schematic of the fabricated cross-sectional transistor structure is illustrated in Fig. 1. The TiN ring gate blocks the high energy Si^{29} implant from getting into the channel region. The area without TiN was implanted with Si^{29} to form *n*+ source and *n*+ drain upon doping activation. The $Ga_2O_3(Gd_2O_3)/Si_3N_4$ dual-layer dielectric film plays an important role to cover the whole wafer and thus unpinned/passivated the entire $In_{0.18}Ga_{0.82}As$ surface. It also serves as an implant activation encapsulation as ensured with the high-temperature thermodynamic stability between the dual-layer dielectric films and $In_{0.18}Ga_{0.82}As$. Ni–Ge–Au (50 Å/125 Å/500 Å) was deposited after wet-etch removal of the dual-layer dielectric in the source/drain regions with buffered-oxide-etch (BOE, 5:1, for Si_3N_4) and HCl [3:1, for $Ga_2O_3(Gd_2O_3)$] solutions to achieve Ohmic contact. This self-aligned process proves to be very effective in minimizing process impact on the dual-layer gate dielectric and its interface with the underlying $In_{0.18}Ga_{0.82}As$.

Figure 2 is a high-resolution transmission electron microscopy (HRTEM) micrograph showing the $Si_3N_4/Ga_2O_3(Gd_2O_3)$ dual-layer gate dielectric stack on $In_{0.18}Ga_{0.82}As/GaAs$. The interfaces of $Si_3N_4/Ga_2O_3(Gd_2O_3)$ and $Ga_2O_3(Gd_2O_3)/InGaAs$ remained atomically sharp after annealing. There is room for further reduction of $Ga_2O_3(Gd_2O_3)$ and thus EOT scaling. Pinhole-free Si_3N_4 with only 2.3 nm thickness is seen on top of $Ga_2O_3(Gd_2O_3)$, contributing ~1 nm to the EOT. HRTEM specimens were prepared with mechanical polishing, dimpling, and ion milling using a Gatan precision ion polishing system operated at 4 keV. The analytical work of TEM sample was performed using a Philips JEOL 2100F-type TEM.

Figures 3 and 4 are the *C-V* characteristics of the $TiN/Si_3N_4/Ga_2O_3(Gd_2O_3)/p\text{-}In_{0.18}Ga_{0.82}As$ MOS structure, with Fig. 3 showing a set of *C-V* curves measured at 1 kHz to 1 MHz from a MOSFET. From the *C-V* data, the EOT of the dual-layer gate dielectric is calculated to be ~5 nm, which is consistent with the EOT estimated from the physical thickness of Si_3N_4 and Ga_2O_3 (Gd_2O_3), as measured from the cross-sectional HRTEM micrograph and their respective κ values. A *C-V* inversion in low frequency *C-V* curves was observed. The measured *C-V* inversion confirms the channel inversion characteristics when $Ga_2O_3(Gd_2O_3)$ was used as the gate dielectric, as reported earlier.[8,9] Figure 4 is the *C-V* measurement with biasing voltages ramping up and down, showing a hysteresis of 100 mV. For a gate dielectric with a total of 5 nm EOT, this is a reasonable number, indicating a small overall bulk trap density in the dual-layer $Si_3N_4/Ga_2O_3(Gd_2O_3)$ gate dielectric stack.

The fabricated MOSFETs were characterized by using HP 4156 semiconductor parameter analyzer. The source and substrate were grounded, the drain voltage V_d was ramped from 0 to +1 V, and the gate voltage V_g was varied from 0 to +4.5 V in steps of 0.5 V. Figure 5 is a set of I_d-V_d

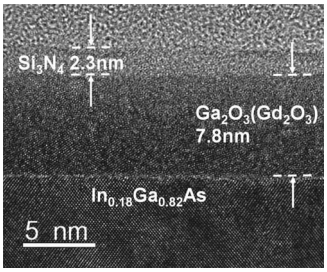

FIG. 2. HRTEM micrograph showing $Si_3N_4/Ga_2O_3(Gd_2O_3)$ dual gate dielectric stack on $In_{0.18}Ga_{0.8}As$ after 600 °C, 15 min annealing in N_2 and then 375 °C, 1 min annealing in forming gas.

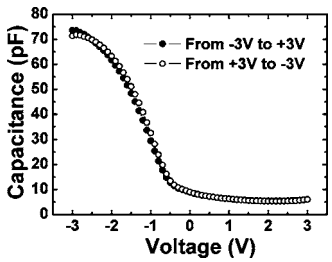

FIG. 4. *C-V* hysteresis measured at 100 kHz, with forward bias ramping from −3 to +3 V and then reverse bias from +3 to −3 V, after stress at +3 V for 30 s with light illumination.

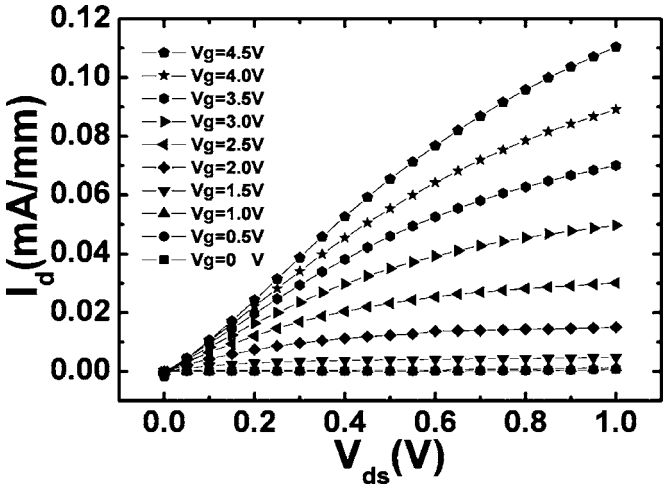

FIG. 5. I_d-V_d curves at various V_g (from 0 to +4.5 V) for an $In_{0.18}Ga_{0.82}As$ MOSFET with $Si_3N_4/Ga_2O_3(Gd_2O_3)$ as dual gate dielectric. The gate length L is 10 μm and gate width is 880 μm.

transfer characteristics of a MOSFET with a gate length of 10 μm and a gate width of 880 μm. I_d of 0.1 mA was measured at V_g of 4.5 V and V_d of 1 V, which is comparable to the previously published results on inversion-channel MOSFET based on GaAs substrate;[10] for example, I_d=0.12 mA of a 1 μm gate length $Al_2O_3/In_{0.2}Ga_{0.8}As/GaAs$ MOSFET with the gate dielectric deposited by an atomic layer deposition was reported.[4] The I_d-V_d transfer characteristics are of a typical enhancement mode MOSFET with channel inversion, indicating the unpinning of $In_{0.18}Ga_{0.82}As$ surface Fermi level.

In conclusion, we have developed a moisture resisting and thermally stable Si_3N_4/Ga_2O_3 (Gd_2O_3) dual-layer gate dielectric on $In_{0.18}Ga_{0.82}As$ for enhancement mode MOSFET with channel inversion application. A total of 5 nm EOT in the $Si_3N_4/Ga_2O_3(Gd_2O_3)$ dual-layer gate dielectric approach was achieved, with the Si_3N_4 contributing to an ~1 nm impact on EOT. We have further demonstrated a working enhancement mode $In_{0.18}Ga_{0.82}As$ MOSFET with channel inversion to show that $Si_3N_4/Ga_2O_3(Gd_2O_3)$ functions effectively in unpinning $In_{0.18}Ga_{0.82}As$ surface Fermi level. Further scaling of EOT is possible when we use thinner $Ga_2O_3(Gd_2O_3)$ and apply dielectrics with higher κ value than that of Si_3N_4 on top of $Ga_2O_3(Gd_2O_3)$.

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