## 國立清華大學命題紙

98 學年度\_奈米工程及微系統\_(所)\_\_\_\_\_\_\_\_组碩士班入學考試

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- 1. Answer the following questions:
  - a) List the characteristic of an ideal OP Amp. (3%)
  - b) What is the meaning of CMRR? What is the effect of CMRR? (3%)
  - c) What is the channel-length modulation in MOSFET? What is its effect in operating MOSFET? (3%)
  - d) What is the Miller's capacitance? What is its effect for 3-dB frequency? (3%)
  - e) Comparing the voltage gain, input resistance, and output resistance among common-source amplifier, common-gate amplifier, and source-follower amplifier. (3%)
- 2. For the circuit shown in Figure 2, derive the output function  $V_o(s)$  in terms of the passive elements and the input voltages. (15%)

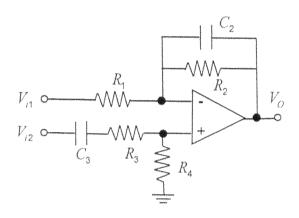


Figure 2

3. The diodes in the circuit shown in Figure 3 have the constant voltage drop ( $V_D = 0.7 \text{ V}$  with no internal resistance). Determine the output voltage  $V_o$  and the currents  $I_{DI}$ ,  $I_{D2}$ ,  $I_{D3}$ , and I for the inputs  $V_I = 4 \text{ V}$  and  $V_2 = 1 \text{ V}$ . (10%)

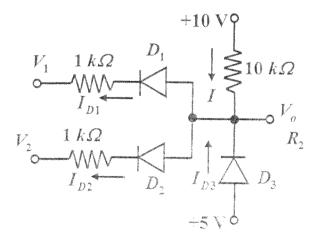


Figure 3

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### 科目 電子學 科目代碼 1806 共 3 頁第 2 頁 \*請在【答案卷卡】內作答

- 4. For the amplifier shown in Figure 4, the internal capacitances of the transistors are neglected.
  - (a) Draw the small-signal equivalent circuit for the amplifier. (3%)
  - (b) Use the small-signal equivalent circuit in part (a) to derive the expression for the input resistance

 $R_{in}$  and the voltage gain  $v_o / v_{sig}$  of the circuit. (12%)

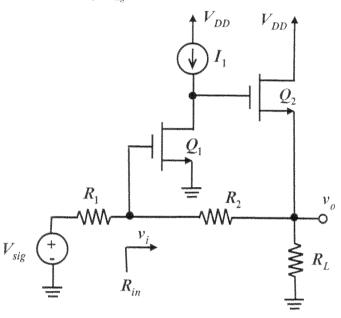


Figure 4

- 5. The BJT common-emitter amplifier of Figure 5 includes an emitter degeneration  $R_{E}$ .
  - (a) Assume that  $\beta$  is very large, the current source I is ideal, and  $r_o$  and  $r_x$  are neglected. Derive an expression for the small-signal voltage gain  $A(s) = V_o/V_{sig}$  that applies in the midband and the low frequency band. (10%)
  - (b) Use the results of part (a) to find the midband gain  $A_M$  and the lower 3-dB frequency  $f_L$ . (5%)

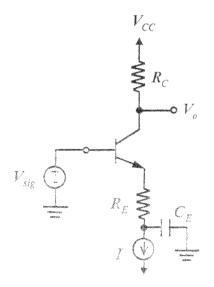
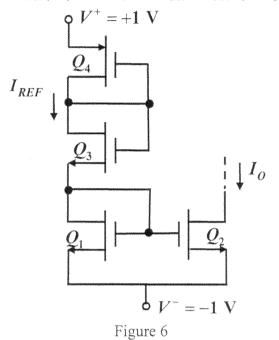


Figure 5

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6. The parameters of the transistor circuit in Figure 6 are  $V_{tn} = +0.3 \text{ V}$ ,  $V_{tp} = -0.3 \text{ V}$ ,  $\mu_n C_{ox} = 80 \text{ } \mu\text{A/V}^2$ ,  $\mu_p C_{ox} = 40 \text{ }\mu\text{A/V}^2$ , and  $\lambda_n = \lambda_p = 0$ . Design the circuit (finding the W/L ratio for each transistor) such that  $I_O = 16 \mu A$ ,  $I_{REF} = 32 \mu A$ ,  $V_{DS2}(\text{sat}) = 0.2 \text{ V}$ , and  $V_{GS3} = V_{SG4}$ . (15%)



7. Figure 7 shows a differential cascade amplifier with an active load formed by a Wilson current mirror. Assuming all transistors to be identical, show that the differential voltage gain  $A_d$  is given by

$$A_d = \frac{1}{3}\beta g_m r_o \quad (15\%)$$

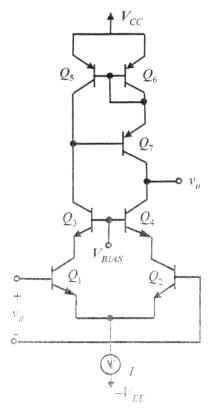


Figure 7