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Fabrication and characterization of metal-ferroelectric (PbZr0.53Ti0.47O3)-insulator (Dy2O3)-semiconductor capacitors for nonvolatile memory applications

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Metal-ferroelectric-insulator-semiconductor capacitors with Pb(Zr0.53,Ti0.47)O3 (PZT) ferroelectric layer and dysprosium oxide (Dy2O3) insulator layer were fabricated and characterized. The measured memory window of 0.86 V was close to the theoretical value \( \Delta W \approx 2d/e_r \approx 0.78 \) V at a sweep voltage of 8 V. The size of the memory window as a function of PZT film thickness was discussed. The C-V flatband voltage shift \( (\Delta V_{FB}) \) as a function of charge injection was also studied. An energy band diagram of the Al/PZT/Dy2O3/p-Si system was proposed to explain the memory window and flatband voltage shift. The charge injection is mainly due to electrons. © 2006 American Institute of Physics. [DOI: 10.1063/1.2177549]

Recently, ferroelectric memory field effect transistors (FEMFETs) with a metal-ferroelectric-insulator-silicon (MFIS) structure have emerged as promising nonvolatile memory devices. The superior characteristics of MFIS include a single-device structure, low power consumption, and nondestructive readout operation. However, before they can be utilized, the electrical properties of MFIS capacitors such as memory window and leakage current need to be better understood. In the literature, the investigated ferroelectric layers in the MFIS structure include SrBi2Ta2O9 (SBT), Pb(Zr0.53,Ti0.47)O3 (PZT), and the insulator layers include SiO2, Si3N4, Al2O3, ZrO2, TiO2, MgO, and Y2O3. The purpose of the insulator layer is to prevent the reaction and interdiffusion between the ferroelectric layer and silicon substrate, as well as to improve the retention properties. Although good interface properties of SiO2/Si can be achieved in the MFIS structure using PZT as the ferroelectric layer, it is difficult to apply sufficient voltage to the PZT layer because the dielectric constant of PZT is much higher than that of SiO2. High-\( k \) insulator layer is attractive because proportionally larger voltage can be applied across the ferroelectric layer.

High-\( k \) lanthanide oxides are good candidates for gate dielectrics. Some lanthanide oxides such as La2O3, Gd2O3, Lu2O3, and Dy2O3 are thermodynamically stable in contact with Si. Another key criterion for the selection of high-\( k \) dielectric is the band offset. A dielectric with large band offset will give high energy barriers for electrons and holes. The energy band gap of Dy2O3 is 4.8 eV. In this work, the thickness of PZT layer was varied from 200 to 260 nm and the thickness of the Dy2O3 layer was 20 nm. The size of the memory window was investigated by the capacitance-voltage (C-V) method. The memory window as a function of ferroelectric film thickness was discussed. The energy band diagram of the MFIS structure is constructed to explain the experimental results.

\( P \)-type (100) orientation, 4-in. diameter silicon wafers (6.5–8 \( \Omega \) cm) were used as the starting substrates. The Dy2O3 and PZT thin films were deposited by rf magnetron sputtering at room temperature. The PZT target was Pb0.1(Zr0.53,Ti0.47)O3. The excess of Pb was to compensate volatile PbO. A thermal treatment was performed for PZT in pure O2 at 700 °C for 60 s. The crystalline phase of PZT thin films was identified by x-ray diffraction (model Shimatzu XD-5). The aluminum electrode was patterned using a lift-off process. Postmetallization annealing (PMA) was performed at 400 °C in N2 ambience for 30 s. The C-V characteristics were measured with an HP4284B LCR meter. The area of the capacitors is 150 \( \times \) 150 \( \mu \)m. The interface-trapped density \( (D_i) \) of Al/PZT/Dy2O3/Si capacitors using the conductance method is \( 3 \times 10^{11} \) eV\(^{-1} \) cm\(^{-2} \). The relative dielectric constant \( \varepsilon_r \) of PZT and Dy2O3 obtained from separate Au/PZT/Pt (MIM) and Al/Dy2O3/Si (MIS) capacitors is 500 (Ref. 18) and 14, respectively. Figures 1(a) and 1(b) show the secondary-ion-mass spectroscopy (SIMS) profiles of as-deposited and 700 °C-annealed PZT/Dy2O3/Si samples. It is clear that the out-diffusion of Pb, Zr, and Ti atoms is contained within the Dy2O3 layer. Thus, the Dy2O3 insulator serves as a good barrier layer to suppress Pb diffusion into silicon substrate.

FIG. 1. (a) SIMS profiles of as-deposited and (b) 700 °C annealed PZT/Dy2O3/Si MFIS samples.
Figure 2 shows the C-V memory windows of MFIS capacitors with different PZT film thicknesses. The theoretical memory window is \( \Delta W = 2d_i E_c \).\(^1\) The voltage drop across the ferroelectric layer (\( V_f \)) and the insulator layer (\( V_i \)) can be expressed as \( V_f = E_d d_f e_f \) and \( V_i = E_i d_i e_i \), where \( d_f \), \( d_i \), \( e_f \), and \( e_i \) are the film thicknesses and the dielectric constants of the ferroelectric and the insulator layers, respectively. For a PZT thickness of 230 nm, the \( V_f/V_i \) ratio is about 230 \( \times \) 14/20 \( \times \) 500 = 1:3. Therefore, the voltage across the PZT layer is given by about one-fourth of the total applied voltage. For an applied voltage of 8 V, 2 V is applied across the PZT layer. The electric field across the PZT layer is about 90 kV/cm. From our previous Au/PZT/Pt capacitor result, the remnant polarization (\( P_r \)) and the coercive field (\( E_c \)) under the electric field of 90 kV/cm are 2.9 \( \mu \)C/cm\(^2\) and 16.8 kV/cm, respectively. The memory window can thus be calculated as \( 2d_i E_c = 0.78 \) V, which is close to the measured memory window of 0.86 V. The dependence of the memory window on the thickness of the ferroelectric layer and the insulator layer was discussed in our previous work\(^2\) and can be obtained using the following equations:\(^1\)

\[
E_f = \left( \frac{e_f}{e_f d_f + e_i d_i} \right) \cdot V_G, \tag{1}
\]

\[
E_i = \left( \frac{e_i}{e_f d_f + e_i d_i} \right) \cdot V_G, \tag{2}
\]

where \( E_f \) and \( E_i \) are the electric fields in the PZT layer and Dy\(_2\)O\(_3\) layer, respectively. \( V_G \) is the gate voltage. In the present case, the memory windows decrease slightly with decreasing PZT thickness under the same sweep voltage. This is because the electric field \( E_i \) in the insulator layer is increased with decreasing \( d_f \). As a result, the charge injection effect is enhanced.

The C-V orientation is influenced by two effects, the polarization of the ferroelectric layer and the trapped charges injected into the insulator layer. When a negative voltage is first applied to the gate of the MFIS capacitor, the PZT layer becomes polarized and an extra number of positive charges will be induced at the silicon surface due to the polarization of the PZT layer. When the sweep voltage increases from negative to positive voltages, an additional positive voltage is needed to convert the silicon surface from accumulation to inversion. Thus, the C-V curve is shifted toward the right. The reverse is true when the sweep voltage changes from positive to negative. Hence, there will be a clockwise C-V hysteresis window. This is the polarization effect. Figure 3 shows that the C-V curves are shifted toward to the right (positive\( \Delta V_{FB} \)) when the swept voltage changes from negative to positive, which indicates that the dominant mechanism is ferroelectric polarization.

When the voltage sweeps from positive to negative, the polarization effect should give a negative\( \Delta V_{FB} \). However, Fig. 3 shows that most of the \( \Delta V_{FB} \) are positive. This is due to the charge injection effect. When a negative bias is initially applied on the Al electrode, some positive charges will be injected into and trapped in the insulator layer, which in turn induces negative charges in the silicon surface. When the applied voltage sweeps from negative to positive voltage, the positive voltage needed to convert the silicon surface from accumulation to inversion will become lower. Thus, the C-V curve is shifted toward the left. The reverse is also true. Therefore, the effect of the injected electron charges is to make the C-V orientation counterclockwise. The samples with thicker PZT of 260 nm show negative \( \Delta V_{FB} \) from polarization effect, whereas the thinner ones show positive\( \Delta V_{FB} \). The charge injection effect is lesser for larger \( d_f \) and therefore lesser \( E_i \).

Figures 4(a) and 4(b) show the energy band diagrams of the Al/PZT/Dy\(_2\)O\(_3\)/Si MFIS structure under negative and positive to negative. Hence, there will be a clockwise C-V hysteresis window. This is the polarization effect. Figure 3 shows that the C-V curves are shifted toward to the right (positive\( \Delta V_{FB} \)) when the swept voltage changes from negative to positive, which indicates that the dominant mechanism is ferroelectric polarization.

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positive gate biases, respectively. The energy band gap of Dy₂O₃ is 4.8 eV.¹⁴ The Al/Dy₂O₃ barrier height was calculated from Schottky emission to be 0.89 eV.²⁰ The Dy₂O₃/Si barrier height can then be calculated as 0.79 eV. The energy barrier for holes at the Dy₂O₃/Si interface is thus 2.91 eV. An electron affinity of 3.26 eV for Dy₂O₃ is obtained. Taking the work function of Al as \( \Phi_{Al} = 4.15 \) eV, the electron affinity of PZT is 2.15 eV and the energy band gap of PZT is 3.4 eV, and the barrier height at the Al/PZT interface \( \Phi_{Al/PZT} \) is about 2.0 eV for electrons and 1.4 eV for holes. Since the electron barrier height at the Dy₂O₃/Si interface is the smallest one, the charge injection is mainly due to electrons.

In summary, Al/PZT/Dy₂O₃/Si MFIS capacitors were fabricated and characterized. The \( C-V \) memory window of 0.86 V is consistent with theoretical estimate. The size of the memory window is measured as a function of PZT film thickness. The memory window is also affected by charge injection. An energy band diagram of the Au/PZT/Pt system is proposed to explain the memory window and flatband voltage shift (\( \Delta V_{FB} \)). The charge injection is mainly caused by electrons.

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