Hybrid Integration of Electrical and optical interconnects

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ABSTRACT

In this paper, we describe a novel approach for fabrication of low-cost optoelectronic modules for optical interconnect applications. The concept includes, (a) placement of optical and electrical components on a common substrate using a chip-first MCM structure to improve thermal handling capabilities, (b) fabrication of both optical and electrical interconnects using planar processes compatible to standard IC processes in manufacturing to reduce nonrecurring engineering (NRE) costs, and (c) application of adaptive interconnect for device-to-waveguide alignment to reduce recurring packaging costs. Preliminary results on waveguide fabrication and modeling of adaptive interconnect are discussed in this paper.

1. INTRODUCTION

The rapid growth in tele- and data-communication have significantly increased the demand for data transmission capacities at all levels of communication systems from long haul, local loops, to cabinet-to-cabinet, board-to-board, and module-to-module. In spite of the fact that optical interconnect (e.g. fiber optics) has successfully demonstrated both performance and cost advantages in long haul telecommunication systems, its acceptance as the preferred interconnect technology in computer systems has progressed very slowly. To a large extent, this is due to the

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incompatibility between packaging technologies of optoelectronic devices developed mostly for the telecommunication industry and those of electronic devices in today's high-performance and high-density digital systems used by most computer manufacturers.

As the performance of IC chips and modules continue to improve with clock speeds over several hundred MHz (Mbs), performance improvements for future products using optical interconnects will become increasingly important and the optoelectronic packaging cost is a dominant factor that determines user acceptance. Development of any low-cost optoelectronic packaging technology must be able to reduce both nonrecurring and recurring engineering costs of packaging. This will happen if the packaging technology developed for optoelectronic components is compatible with and can leverage on the existing IC processing and packaging technologies. In this paper, we describe an effort of developing a low-cost optoelectronic package technology by hybrid integrating electronic and optoelectronic devices in a multichip module (MCM) and applying standard planar processes for fabrication of both electrical and optical interconnects. The device-to-waveguide alignment is achieved by using an adaptive interconnect technique developed originally for high-density interconnect in electronic MCM packaging.

2. PACKAGING APPROACH AND DESCRIPTION

Because of their ability for handling different types of devices and their compatibility with existing electronic packaging processes and materials, MCMs provide an ideal platform for optoelectronic packaging. In addition, the thin film MCMs processes using polymer as the dielectric layers are compatible with those required for construction of polymer interconnect channels using optical waveguides. Previous workers have demonstrated silica or polyimide optical waveguides on silicon or polyimide substrates to interconnect different devices optically. Self-alignment techniques such as flip-chip and solder-bumps were used for final optical chip placement and packaging. In our approach, several novel features are introduced, and described in the following sections.

(a) A chip-first MCM technology is employed and both electrical and optical components are mounted in contact with the substrate for improving thermal dissipation.
(b) Planar processes are used and both optical and electrical interconnects are made using fully compatible fabrication processes for reducing NRE costs.
(c) Adaptive interconnect is used and the device-to-waveguide alignment is achieved using fiducial marks for reducing recurring packaging costs.
2.1 Chip-first MCM packaging:

Our packaging approach is schematically illustrated in Fig. 1 in which the electronic and optoelectronic devices are hybrid integrated in a thin film multichip module (MCM). The process steps are briefly described as follows.

![Diagram of Chip-first MCM Packaging]

**Key Features:**
- Hybrid MCM Packaging (GE HDI Process)
- Adaptive Interconnect (Al)
- Planar Fabrication Process

2.2 Electronic and optical devices are placed on a common substrate:

In chip-first MCM packaging, both active and passive components are placed inside the cavities milled into a substrate, typically alumina (Al₂O₃) or aluminum nitride (AlN), thus providing good thermal dissipation. This feature is unique in the chip-first MCM configuration and is important for packaging active electrical and optical devices consuming large amounts of power. The interconnection between devices are sequentially fabricated on top of the devices and substrate using planar fabrication processes such as lamination and thin film metallization procedures well developed in IC manufacturing.
2.3 Fabrication of electrical interconnect:

The electrical interconnect is first fabricated using a standard thin film process. In the GE-HDI process, a 25-um thick Kapton film is first laminated over the top of the chips placed inside the chip wells. An argon laser lithography system is used to drill via holes through the Kapton films for making interconnects to the chip I/O pads. The electrical interconnects and via contacts are formed by a combination of sputtering/electroplating and resist patterning processes. After completion of the first layer, the processes are repeated to form the successive interconnect layers. Since all interconnects are formed by planar processes and lithography techniques, good controls of interconnect lines within the module are possible. A cutaway perspective of this MCM structure and a micrograph of the MCM cross-section is shown in Fig. 2.

Fig. 2 - A cutaway perspective of the MCM structure and a micrograph of the MCM cross-section showing a multi-layer polyimide thin film dielectrics with metalized vias. (Single layer thickness is 37-um)
2.4 Fabrication of optical interconnect:

After completion of electrical interconnect, the optical interconnect channel consisting of cladding and core layers is fabricated by successively applying thin polymer films. The optical waveguides are formed by a combination of resist patterning and etching processes similar to those used for electrical interconnect fabrication.

2.5 Adaptive Interconnect for waveguide-to-device alignment:

Alignment between optical interconnect channels (e.g. waveguides) and active devices (e.g. lasers, detectors) is a key problem in optoelectronic packaging and contributes much to the packaging cost in sub-assembled optoelectronic systems. Both active and passive alignments require high-precision machined components and involve serial assembly procedures and discreetly handled parts. All of these procedures and parts contribute to packaging cost. In addition, multi-channel parallel optical links will be required for computer applications and any optoelectronic packaging methods must be scaleable for handling array devices.

In our approach, the alignment between device-to-waveguide is accomplished using an adaptive alignment procedure originally developed for high-density electrical interconnect to accommodate chip misplacement in the MCM process. The adaptive process first locates the actual chip placement position, and an argon laser patterning system, controlled by a proprietary software, is used to pattern interconnect channels adaptively. The actual chip placement is identified using the fiducial marks and can be quickly located.

Fig. 3 illustrates the concept of adaptive alignment between an active device (e.g. a three-channel laser array) and the optical waveguides. The top left figure shows the design position in which the device is aligned properly to the waveguides, while the top right shows the actual device location in which the laser array is positioned slightly downward. In this case, the device fiducial marks are registered and the laser is directed to pattern the waveguide channel adaptively, as shown in the top right figure. The bottom figure shows a representative waveguide pattern fabricated using the adaptive lithography method described above.
Fig. 3 - The concept of adaptive alignment between an active device (e.g. a three-channel laser array) and the optical waveguides is illustrated schematically (Top photos), and a micrograph shows an adaptive waveguide pattern fabricated using this technique (Bottom photo).

To calculate the coupling loss introduced by the adaptive interconnected path, a 2D waveguide model was employed to determine the propagation loss in a multi-mode polyimide waveguide using the following parameters: Wavelength = 0.83 μm, waveguide width (W) = 25 μm, adaptive offset (d) = 20 μm, adaptive length (Z) = 500 μm, and core index = 1.55, and cladding index = 1.50 (defined in Fig. 4), the propagation loss calculated as a function of the propagation distance is shown in the figure for waveguides with three different degrees of edge smoothness. This preliminary result shows the loss can be minimized by properly designed system parameters.

**Modeling of Propagation Loss in a Multimode Polyimide Waveguide**

**Parameters:**
- 2D step index model
- Wavelength = 0.83 μm
- W = 25 μm, d = 20 μm, Z = 500 μm
- Waveguide index, n, = 1.55, and n, = 1.50
- Bend angle = \( \tan^{-1}\left(\frac{d}{Z}\right) \)
- Critical angle = 14.8 degree

![Modeling of Propagation Loss](image)

Fig. 4 - Modeling of propagation loss in a multimode waveguide with adaptive interconnect section.
3. SUMMARY:

In summary, we describe in this paper a novel approach for low-cost packaging of optoelectronic devices. The concept includes the placement of optical and electrical components on a common substrate using a chip-first MCM structure to improve thermal handling capabilities. Fabrication of both optical and electrical interconnects are achieved using planar processes commonly employed in IC manufacturing to reduce NRE costs. In addition, an adaptive interconnect scheme is employed to achieve device-to-waveguide alignment, and reduce alignment costs. Our results on waveguide fabrication and modeling of adaptive interconnect coupling losses are discussed and have demonstrated the feasibility of this approach.

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