行政院國家科學委員會專題研究計畫　成果報告

整合型 CMOS 低噪聲微振動感測晶片之設計與製作

計畫類別：個別型計畫
計畫編號：NSC92-2212-E-007-042-
執行期間：92 年 08 月 01 日至 93 年 07 月 31 日
執行單位：國立清華大學電子工程研究所

計畫主持人：盧向成

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自動化學門專題計畫

(Development of an Automatic)

計畫編號：NSC 99－1111-E-001-001

執行期限： 92 年 8 月 1 日至 93 年 7 月 31 日

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一、中文摘要

我們提出設計及製作一新穎 具低噪聲 μg 解析度的微加速度計，與同感測度的加速度計比較，其特色在於其更微小化的體積。我們將使用 CMOS 微機電技術完成感測器及電容式感測電路的直接整合、以大幅降低非直接整合時所帶來的大量寄生電容。一特殊 CMOS 相容的體加工方式可製作高深寬比結構及感測電極以提昇感測度；並且利用靜電的軟化彈簧效應配合穩定迴授控制，更增加感測度以達到μg 解析度目標。

關鍵詞：μg-加速度計、CMOS 微機電、高深寬比活性離子蝕刻、低噪聲電容式感測。

Abstract

We propose to design and fabricate a novel low-noise accelerometer with a μg resolution, which compares favorably with other low-g inertial sensors in its small size. The CMOS-MEMS technology is used for monolithic integration of the sensor and the capacitive readout, in order to minimize the parasitic capacitances if implemented otherwise. A special CMOS-compatible bulk micromachining process helps to promote the capacitive sensitivity with the resultant thicker micromechanical structures. Additional sensitivity increase is obtained via the use of a feedback control scheme, in which the accelerometer is operated in a spring-softening regime and stabilized in a controlled loop.

Keywords: μg-Acclerometer, CMOS-MEMS, Deep reactive ion etch, Low-noise capacitive sensing.

二、計畫緣由及目的

The goal of this project is to fabricate an ultra-sensitive accelerometer whose resolution is in the sub-μg resolution, namely, close to what is required for seismic measurements. In addition to the low-g performance, we emphasize that the device comes with a small feature size in a few hundred microns. Such a device is at least one to two orders of magnitude smaller than existing devices having the same resolution, indicating that, with great sensing capability and miniaturized size, this type of inertia senor can be collectively deployed for distributed sensing of environment, seismic and geophysical measurement [1], and monitoring of machinery [2]. Academic-wise, we believe that a micromachined ultra low-g inertia sensor is a challenging and synergetic research topic that has to be worked simultaneously from the aspects of micro-fabrication, low-noise readout, and design.

In the past ten years, extensive research effort has been invested in the making of micromachined inertial sensors, such as accelerometers, which are now widely deployed in cars for air-bag triggering or suspension control. Among those most are fabricated by the surface-micromachining technique. For example, the ADXL 105 accelerometer from the Analog Devices, Inc. has an equivalent noise level of 225 μg/√Hz, and the other from UC Berkeley by Lemkin also has similar noise level at 110 μg/√Hz. Due to the limited proof mass and the thin sensing electrode, and what is more, the parasitic capacitance, the design of a μg

surface-micromachined accelerometer is a very challenging issue. The best result, to our best understanding, is a CMOS-MEMS accelerometer from Carnegie Mellon University with a noise acceleration at 50 μg/√Hz [3]. In [3] the total sensing capacitance is less than 100 fF, and the parasitic capacitance is greatly reduced with the substrate under the sensor being removed; in addition, the front-end capacitive readout adopts an open-loop design that features a low input capacitance for sensitivity/noise optimization.

Accelerometers fabricated by the bulk-micromachining technique have shown μg resolution [4] as the proof mass and the electrode thickness increase. The large device size and the difficulty to integrate the sensing pre-amp are the disadvantages inherited by the bulk-micromachining approach.

We herein propose a new approach to enhance the inertia sensitivity without resorting to a large proof mass (Newton's 2nd law), instead, with focus on reducing the effective spring constant (Hooke's law). Still, in our CMOS-MEMS approach, a specialized bulk-micromachining is applied to increase the proof mass and electrode thickness, in an effort to keep a reasonably small sensor size around a few hundred microns on a side.

三、研究方法

Following the end of Section II, the effective spring constant will be controlled by the electrostatic spring-softening effect, which, as known to the MEMS community, produces pull-in in a parallel-plate electrostatic actuator at one-third of the initial gap, at which the mechanical spring constant is negated to zero by the electrostatic force gradient. In our scheme, the effective spring constant will be reduced to around 0.01 N/m, about three to four orders of magnitude smaller than the original mechanical spring. The key to the success would need a feedback loop around the accelerometer to first bring it near the pull-in point for spring softening. Then the controller stabilizes the accelerometer around the operating point when facing the external force. A large controller gain increases the measuring dynamic range, while reducing the sensor output at the same given force. Therefore for ultra-sensitive applications, we would opt to use a small open-loop gain, or even disconnect the feedback loop at the operating point. The control system configuration, as shown in Fig. 1, uses a low-speed pre-filter to slowly bring close the actuation electrodes, in order to avoid unwanted overshoot.

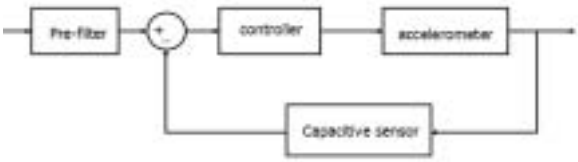

Figure 1: Control system configuration around the accelerometer.

The CMOS-MEMS micromachining process is used to achieve monolithic integration with minimum parasitic capacitance, which, in a hybrid scheme, can easily rise to several pico-farads due to routing leads and wire-bonding pads. These parasitic effects can lead to signal attenuation/noise amplification in an open/closed-loop front-end capacitive readout. As a comparison, in our CMOS-MEMS process, the resultant parasitic capacitances are estimated around tenths of femto-farads.

The process flow in cross-sectional view is depicted in Fig. 2. The tsmc 0.35-μm 2-polysilicon-4-metal mixed-mode CMOS process is used for design and fabrication. After the completion of CMOS, we first perform a back-side anisotropic silicon etch down to about 100-mm thick in an inductively-coupled-plasma (ICP) chamber using SF_6 plasma. Hand-painted photoresist is used as the etch-resistant mask. Following that, an optional electroplating step can add to extra inertia mass, if necessary. Then the front-side dielectric reactive ion etch using top metal as the etch mask is performed until the silicon substrate is exposed, followed by the anisotropic silicon etch for structural release. The released electrode shows that all four metals and the substrate are tied together for capacitive sensing and actuation. Note that for the silicon underneath each finger to be isolated

from the bulk assigned for V_{ss} (circuit bias), that will require an additional isotropic etch using XeF_2 to cut away the silicon under the respective junction. Those junctions have a narrower width (~ 1 μm) than that of the regular finger electrode for easy removal of the underneath silicon; to prevent an incomplete silicon etch, a n-well is placed right underneath the narrow junction and biased positively with respect to the p-type substrate, in order to stop any current flowing from the adjacent silicon.

For a common 40:1 deep reactive ion etch with a 2-μm gap, the thickness of the sensing electrode in Fig. 2(e) can reach 80 μm, which compares no less than what can be achieved by a silicon-on-insulator (SOI) wafer. The main advantage of the CMOS-MEMS approach is that the stray capacitance from the sensing electrode to ground is almost none (no substrate underneath), such that mainly the routing capacitance is considered.

The schematic of the single-axis capacitive accelerometer design is depicted in Fig. 3, in which the springs are shown in light-blue color, the sensing electrodes are in yellow, and the actuation electrodes for spring softening are in red. When an external acceleration is applied, the displacement of the proof mass is converted to that of parallel-plate sensing electrodes, and thus a sensed voltage as shown in Fig. 4. The minimum gap separation is currently chosen as 2 μm, that can be further shrunk down as the high-aspect-ratio silicon etch is available. As we know as of now, 1:70 is available from the Nano Architect Research Corporation in the Industrial Park. The completer design parameters of the accelerometer is listed in Table 1.

The schematic of the capacitive sensing circuit is illustrated in Fig. 5, in which modulation and amplification of the sensed signal is first applied, followed by demodulation and low-pass filtering of the 1x and 2x carrier-frequency signals. The front-end readout uses a two-stage operational op-amp with capacitive feedback. The dc bias at the minus input node of the op-amp is provided by a transistor operated in the sub-threshold region. The demodulation is accomplished by two alternatively operated switches at the carrier frequency to sample the modulated signal,

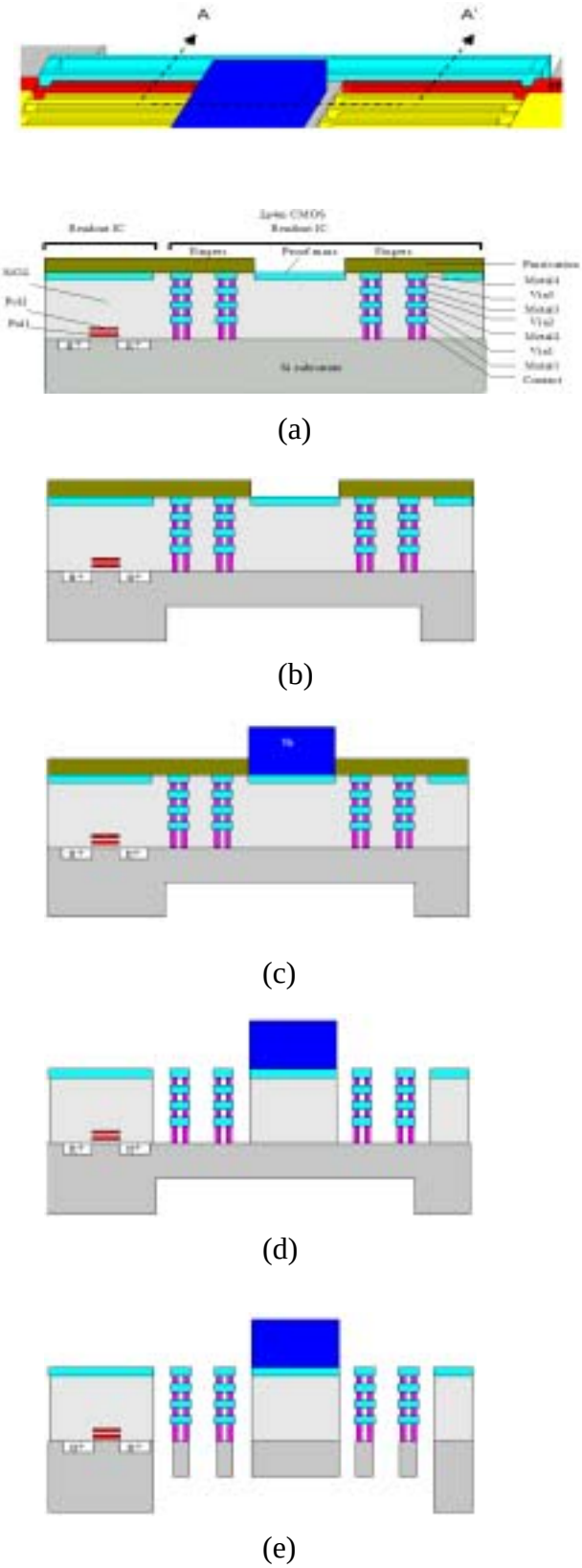

Figure 2: (a) Completion of CMOS. (b) back-side silicon etch. (c) electroplating. (d) front-side oxide etch. (e) front-side silicon release etch.

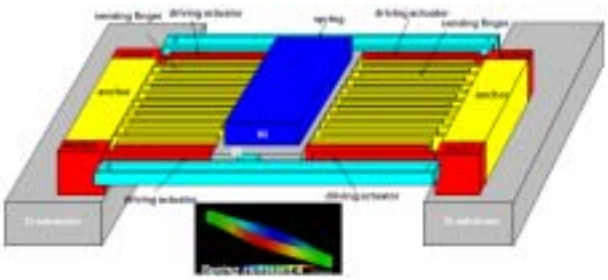

Figure 3: 3D Schematic of the accelerometer.

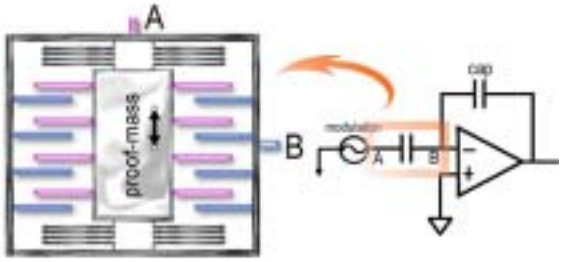

Figure 4: Capacitive sensing of the accelerometer.

Table 1: Design parameters of the accelerometer.

Dimension	650 × 650 μm^2	*driving fingers*	8 pairs
Finger length	200 μm	*sensing finger*	42 pairs
Finger width	5 μm	*Mass*	$4.4*10^{-8}$ kg
Overlap	198 μm	*Resonance*	2.8 kHz
Gap	2 μm	*Sensitivity*	3.33fF/nm
Driving voltage	4.8 V	*Noise*	6 μG /√Hz

followed by a large capacitor for holding the signal. The front-end readout has an output stage that can be measured directly by a spectrum analyzer for the minimum sensing resolution.

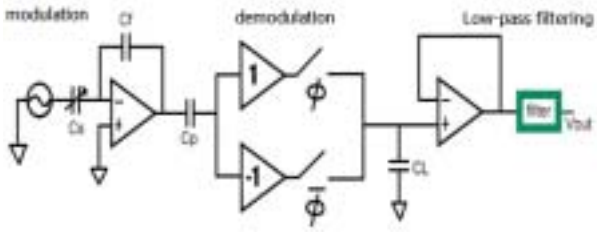

Figure 5: Schematic of the capacitive sensing circuit.

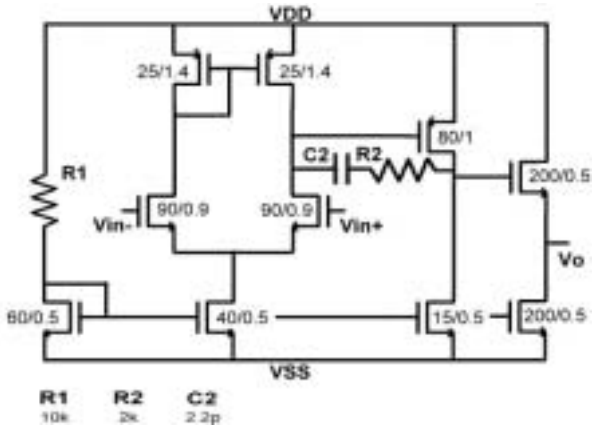

Figure 6: Schematic of the two-stage op-amp for the front-end readout. The transistor sizes in micrometers are illustrated.

The schematic of the two-stage op-amp is shown in Fig. 6. The design achieves an open-loop gain of 68 dB, a unity-gain frequency of 70 MHz, with a phase margin of 60 degrees. All corner simulations have been passed to meet variations in fabrication, as shown by the frequency response of the two-stage op-amp in Fig. 7. The compensating R and C for splitting the two dominant poles are 2 kΩ and 2.2 pF, respectively. A source follower for driving the I/O pad is shown as the last stage.

The total area of the capacitive readout is 260 μm × 150 μm. For test of the complete Figure 8 shows a sinusoidal input that, after demodulation and low-pass filtering, produces a nearly dc demodulated voltage as expected.

Based on the plant parameters given in Table 1, Fig. 9 shows the work of control system simulation in Simulink for pulling the accelerometer close to the pull-in limit. A pre-filter with a pole frequency at 10^4 rad/sec was chosen. The controller was designed with a

proportional gain of 10. The sensing of external acceleration is a disturbance–rejection problem in the simulation. The choice of a larger gain can increase the sensing dynamic range while reducing the sensed output.

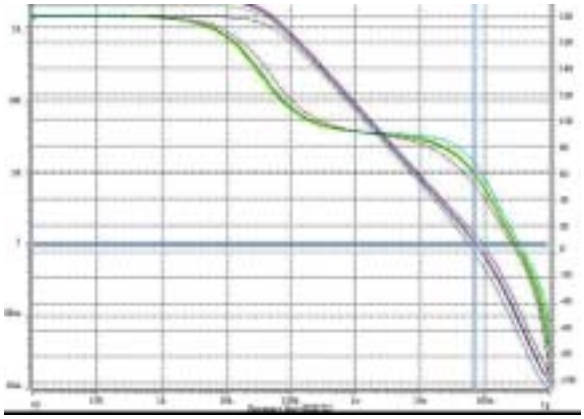

Figure 7: Frequency response of the two-stage op-amp at various corners.

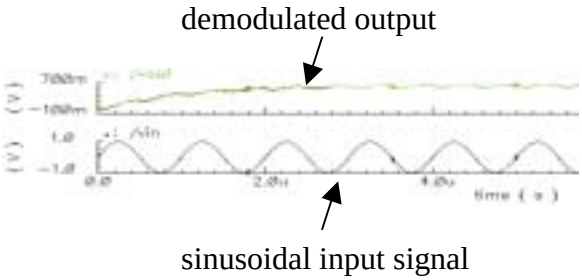

Figure 8: For test of the complete capacitive sensing circuit, a sinusoidal input is applied to produce a dc-like demodulated output as expected.

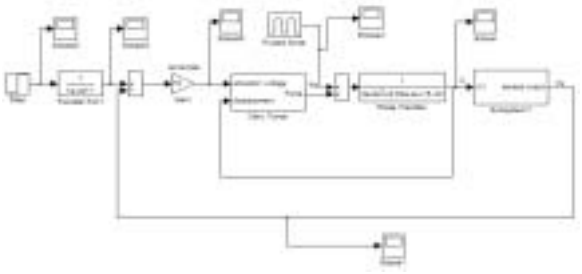

Figure 9: Control system simulation by using the Simulink.

四、結論與成果

The complete layout was submitted in June, 2004, to the tsmc 2P4M 0.35-μm CMOS, and was graded A (highly recommended) in overall review. The chip contains three accelerometer designs, a test circuit, and test structures for measuring structural release. The chip size is 2.2 × 1.8 mm^2.

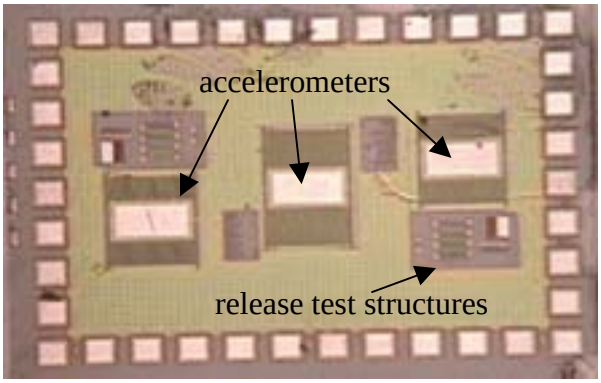

Figure 10: Fabricated die after completion of CMOS.

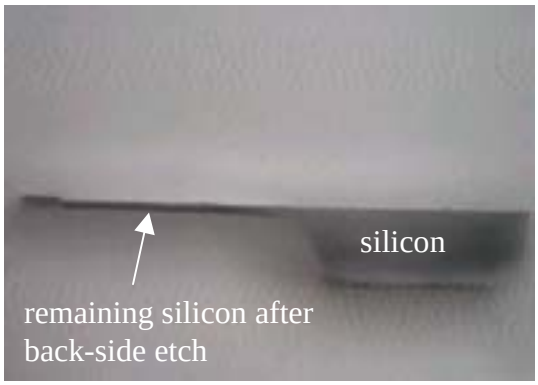

Figure 11: Side view of the CMOS die after the first backside silicon etch. The left side silicon is thinned down to below 100 μm.

The chip was back on September 5, 2004, as shown in Fig. 10. Following the process flow in Fig. 2, we first applied a back-side anisotropic silicon etch down to about 60 – 100 μm thick. A side view of the etched die is shown in Fig. 11. The yield was low at first due to the difficulty of hand-painting the photoresist as the etching mask. The remaining silicon thickness, based on our measurement, varies across four etched dies in 67 μm, 78 μm, 95 μm, and 102 μm. The uneven thickness can be attributed to the varied heat dissipation across dies during

processing. The processing parameters are: coil power = 600 Watts, pressure = 94 mtorr, O_2 = 13 sccm, SF_6 = 130 sccm, DC = 0 V, AC = 155 V, etch rate = 1.2 μm/min.

The front-side anisotropic oxide etch was subsequently applied using the top metal as the etching mask. The processing parameters are: gas = CHF_3, RF power = 90 Watts, flow = 30 sccm, pressure = 1.33 Pa, and etch rate = 22 nm/min. The micrograph after the dielectric etch is shown in Fig. 12. We need to perform another back-side silicon etch to release the structure.

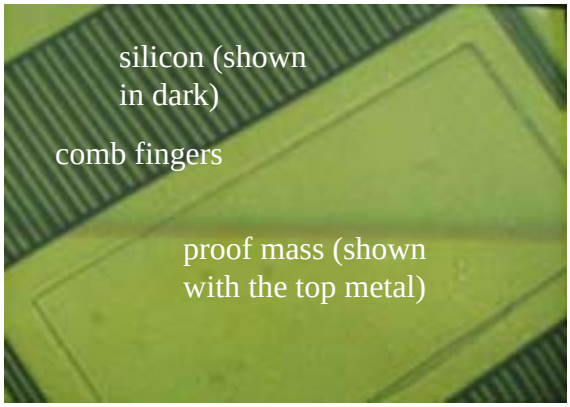

Figure 12: The micrograph of the accelerometer after the dielectric etch.

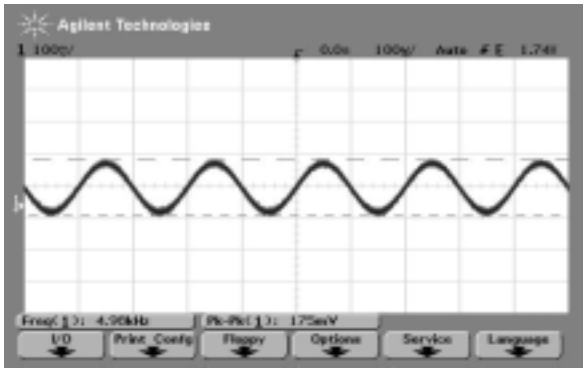

Figure 13: Measured re-amp output to an input signal of 200 mV (peak-to-peak).

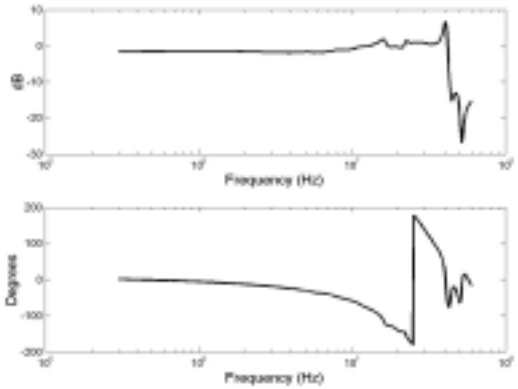

Figure 14: Measured frequency response of the pre-amp test circuit.

The pre-amp shown in Fig. 6 was first tested for its transient and frequency responses. The dc bias at the negative input of the op-amp was provided by a transistor operated in the sub-threshold region. Fig. 13 is the measured pre-amp output to an input signal of 200 mV (peak-to-peak), resulting a measured gain of 0.875. Compared to the expected gain of 1, we believe that the gain reduction was a result of the leakage current due to the relatively low impedance of the sub-threshold transistor with respect to the surrounding capacitances for gain setting. The reason is an error in our design that used a large W/L-ratio transistor instead of a small W/L-ratio one.

The measured frequency response of the pre-amp gain and phase is shown in Fig. 14. The measured -3-dB frequency is close to 40 MHz, less than the 70 MHz predicted by simulation. The reason can be attributed to the large parasitic capacitance seen at the output node.

The progress of this project is a little behind the proposed schedule. Optimistically we would need an additional three weeks to a month to complete the overall test, if the accelerometer can be successfully released.

五、參考文獻

[1] J. Bernstein, R. Miller, W. Kelley, and P. Ward, “Low-noise MEMS vibration sensor for geophysical application,” *J. of Microelectromechanical Systems*, vol.8, no. 4, pp. 433-438, December, 1999.

[2] J. Thomas, R. kuhnhold, R. Schnupp, H.

Ryssel, “A silicon vibration sensor for tool state monitoring working in the high acceleration range,” *Sensors and Actuators A*, 85, pp. 194-201, 2000.

[3] Jengfeng Wu, Sensing and control electronics for low-mass low-capacitance MEMS accelerometers, Ph.D. Thesis, Dept of Electrical and Computer Engineering, Carnegie Mellon University, 2002.

[4] S. Valoff and W.J. Kaiser, “Presettable micromachined MEMS accelerometers,” *Proceedings of the 12th IEEE Int. Conf. on Micro Electro Mechanical Systems (MEMS’99)*, pp. 72-76, 1999.