行政院國家科學委員會補助專題研究計畫成果報告

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※ **由理論模型對毫微點記憶體元件之設計及最佳化研究** ※

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計畫主持人：金雅琴

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□赴國外出差或研習心得報告一份

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行政院國家科學委員會專題研究計畫成果報告
由理論模型對毫微點記憶體元件之設計及最佳化研究
Design and Optimization of Nano-node Memory Device by Theoretical Model

NSC 89－2215－E－007　－045　－
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中文摘要

未來的電子記憶體科技必須要擁有快速的讀寫速度及足夠高的可記憶次數和較為延長的資料儲存時間以作為低功率機動型記憶體的應用，特別是在一些可攜帶型的電子商品。最近，許多研究運用單一電晶體和在二氧化矽閘介電層中毫微點為電荷儲存之地點證明此類型的記憶體較優的特性。在此計劃中，我們提出一個理論模型來了解毫微點記憶體元件特性受到元件各項結構上變數的影響。 半永久型的毫微點記憶體製程上和互補式金氧半元件相容，可作為整合型積體電路之記憶體。 以 Coulomb Blockade 效應為基礎及考量電子穿隧電流的影響，二氧化矽閘介電層中毫微點上的電荷移動的特性，可由提出由理論模型來預估，並對此類型的記憶體的作最佳化的設計。

關鍵詞：電荷儲存、毫微點結構、互補式金氧半元件

Abstract

In this work, the write/erase and retention times of the nano-trap memory device and the impact of nano-trap size and shape are modeled by single charge tunneling theory with Coulomb blockade effect [1]. The feasibility of a nonvolatile device using thin tunnel oxides with 10-year data retention time and 10ns write/erase speed is presented.

Keywords: Nano-crystal, Charge Trapping, Non-Volatile Memory

INTRODUCTION

Future memory technologies require fast write/erase speed, sufficiently high endurance and long refresh time for low-power dynamic application. Table 1 shows the performance of the state-of-the-art memory devices. The single-transistor memory-cell structure with nano-crystal charge-storage sites embedded within the gate dielectric, which has recently been demonstrated [2] represents an interesting new approach. The possibility of exceeding the performance limits of a conventional floating-gate device has spurred many investigations in this area [3]. However, there is no theory available to predict the performance limits or to guide the design of the nano-trap memory devices.

Device	V_{cc}	Write/Erase Time	Data Retention Time	Endurance
DRAM	3V	50~100ns	~ 0.5 sec	No limit
Flash	3V	1ms ~1ms	10 year	10^5

Table 1 Device parameters for different semiconductor memory technologies for either dynamic or non-volatile application.

THEORETICAL MODEL

To simplify the theoretical study, the control oxide thickness is fixed at 50Å and aV_t = 0.5V. Direct tunneling current model is used to estimate the write times. The data retention time, T_r, is defined as when 20% of the stored charge is lost by back tunneling from the floating gate to the channel.

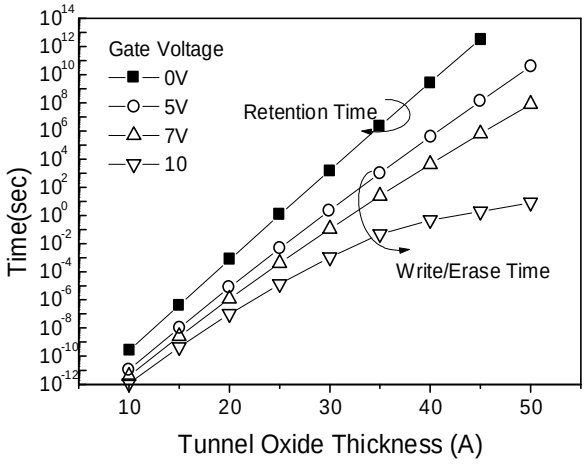

Figure 1 Retention and write/erase times predicted for various write voltages, for the floating gate device. Control oxide is assumed to be 50Å with ΔV_t=0.5V.

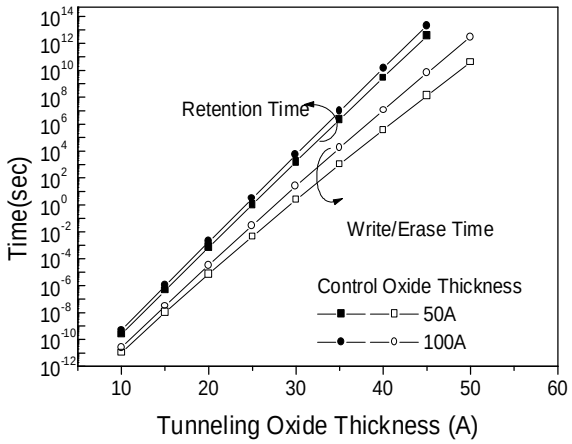

Figure 2 For the floating gate device, a thicker control oxide results in a slightly increased retention time with the tradeoff of a higher write voltage. The write voltage is fixed at 5V.

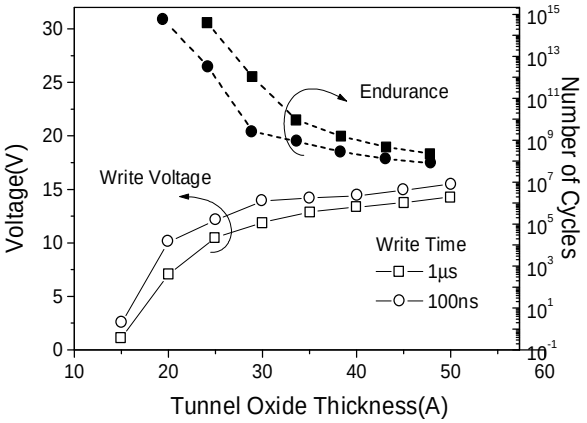

Figure 3 The endurance of the floating gate memory device is greatly increased for thinner oxide thickness.

Fig. 1 shows the write/erase time, retention times of a floating gate memory cell as a function of the tunnel oxide thickness. The write/erase time can reach nano-second range when tunnel oxide is 20Å for a 5V-write voltage. However, the retention time would be only 100µs. Fig. 2 illustrates the tradeoffs between the retention and write times for a thicker control oxide. Using the charge-to-breakdown predicted by the Anode Hole Injection Model [4], the intrinsic endurance at a fixed write speed can be predicted and is shown in Fig. 3. If the tunnel oxide is only 20Å, endurance can be as high as 10^{15} cycles.

For tunnel oxide thicker than 30Å, SILC further degrades the retention time and endurance to below the projection in Fig. 1 and Fig. 3. Although fast write/erase times and high endurance can be achieved by employing a 20Å-tunnel oxide, the retention time is less than a few microseconds.

The dimensions of the trap sites embedded into the gate oxide are extremely small. Charge trapping can be described as single electron tunneling across a very small junction described by the Coulomb Blockade theory [5]. The electron transition probabilities to and off the charge trap sites are:

$$\Gamma^{\pm}(Q) = \frac{\Delta E^{\pm}(Q)}{e^2 R_t [\exp(\Delta E^{\pm}(Q)/k_B T) - 1]} \quad (1)$$

where R_t is the tunneling resistance of the barrier, $aE(Q)$ is the charge electrostatic energy difference when charge in the trap site increases or decreases by one electron and k_B is the Boltzmann constant. The tunneling resistance R_t is modeled as

$$R_t = \frac{2\tau_o}{e^2}\sqrt{\frac{\Phi_b}{m_{ox}}}\exp\left(\frac{\sqrt{2m_{ox}\Phi_b}}{\hbar}d\right)\frac{1}{d}\exp\left(-\sqrt{\frac{m_{ox}}{4\Phi_b}}\frac{ed}{\hbar}V\right) \quad (2)$$

where m_{ox} is the electron effective mass in SiO_2, Φ_b is the barrier height, d is the tunnel oxide thickness, V is the voltage on the tunnel barrier and τ_o is the tunneling time constant[6].

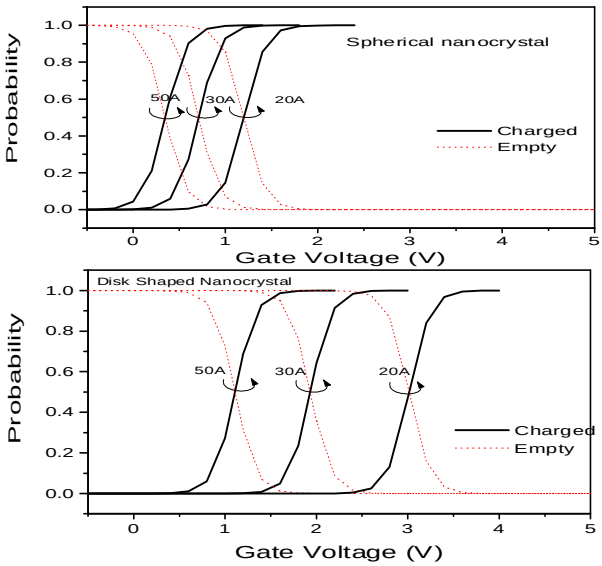

Figure 5 Spherical nano-traps result in larger capacitance, so the write voltages are lower. The tunnel oxide thickness, d, is fixed at 15Å.

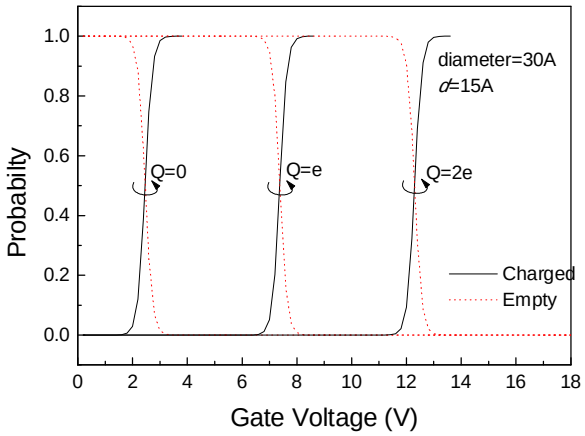

Figure 6 Comparison of the filled and empty probabilities for various pre-existing charges on a disk shape trap

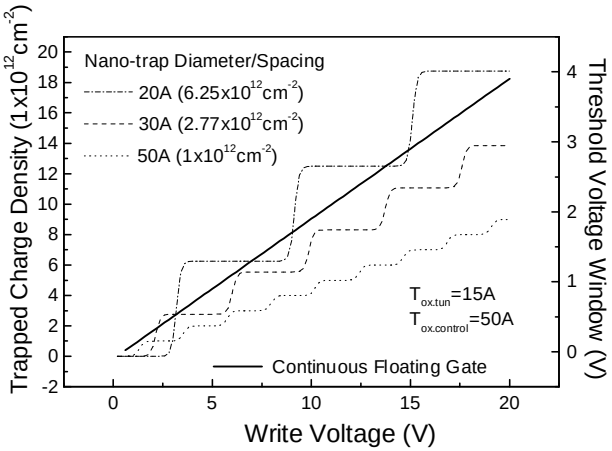

Figure 7 Number of trapped electrons in the nano-traps at steady-state with increasing write voltage.

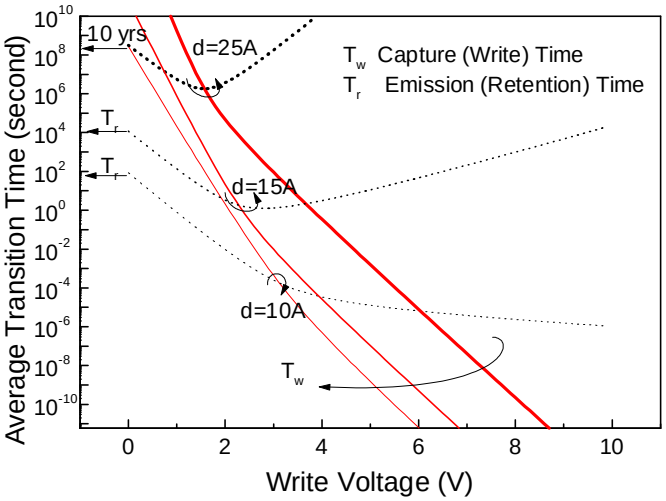

Figure 8 The transition time for the first electron on/off the nano-traps. The tunnel oxide thickness affects the write and retention characteristics drastically.

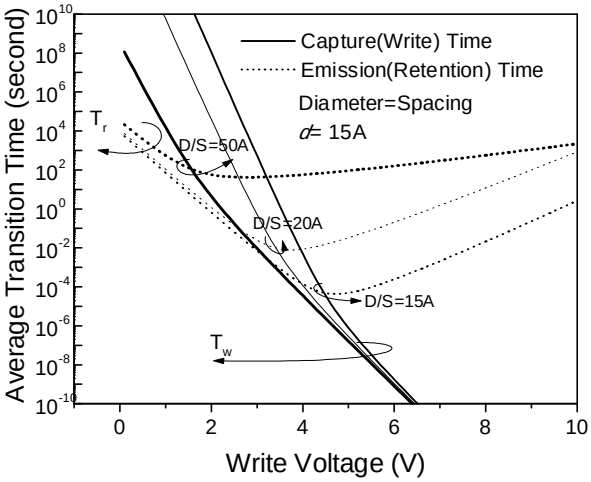

Figure 9 The size of the nano-traps have more effect on write voltage than on the retention and write time.

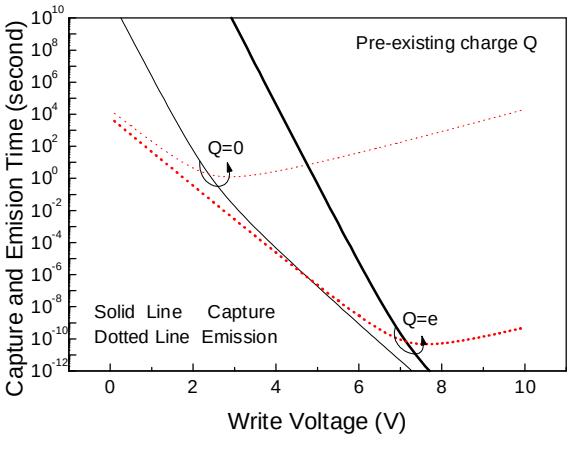

Figure 10 Average capture and emission time for nano-trap with and without pre-existing trap

charge

RESULTS AND DISCUSSION

The write characteristic of the memory device depends on aE through the trap capacitance, which in turn depends on the size and shape of the nano-traps. The probabilities of an electron being captured or released for spherical and disk-shaped nano-traps of various diameters are shown in Fig. 5. A spherical trap-site has larger capacitance, and therefore lower write voltages. Fig. 6 shows that successively higher write voltages are needed to inject a 2^{nd} and 3^{rd} electron into a nano-trap. As shown in Fig. 7, a lower write voltage is needed to place electrons onto a larger trap site. However, the density of stored electrons needed to create the desired threshold shift poses a limit on the maximum size of the nano-traps. To minimize the write/erase voltage, one should choose the largest trap size that provides the desired V_t shift with one trapped electron per site. The write characteristics for various tunnel oxide thicknesses is shown in Fig. 8. The write time is the average capture time at a certain gate bias, whereas the retention time is predicted by the average emission time of the electrons at zero gate voltage. Fig. 9 shows that the retention time increases and write time decreases as the size of the nano- nodes increases, but the effect is weak in the most interesting regimes of long T_r and short T_w.

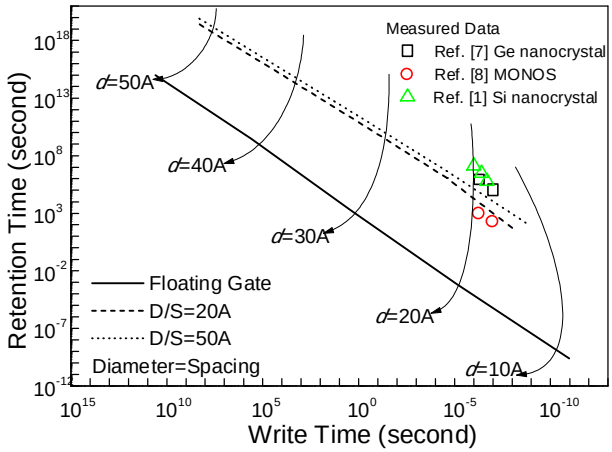

Figure 11 The comparison of write speeds and retention times of nano-trap and floating gate memory models and measured data from previous studies [1,7, 8].

Furthermore, the write and retention times are also affected by the number of pre-existing electron on the traps as illustrated in Fig. 10. Fig. 11 shows that nano-trap memory devices can yield 10^8 times longer retention time than the floating gate device with 10 to 30Å tunnel oxide and that nano-trap memory with 10ns and 10 years retention is possible.

計畫成果自評

In this work, we accomplished our goal of proposing a theoretical model to explain the limitations of nano-trap memory devices using a single electron tunneling model. High speed write and erase and extended retention can be achieved by optimizing the tunnel oxide thickness and size of the nano-traps.
In work have to published in 2001 Device Research Conference, June 24,25 in U.S.A.

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